EE 330
Lecture 18

- P-channel Modeling
- Relationship Between Switch-Level and Higher Level Models
- CMOS Process Flow

Spring 2024 Exam Schedule

Exam 1	Friday Feb 16
Exam 2	Friday March 8
Exam 3	Friday April 19
Final Exam	Tuesday May 7 7:30 AM - 9:30 AM

Prelab Announcement

A Pre-Lab for Lab 7 has been posted on the class WEB site

How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model

Square-law model (with λ and bulk additions)

α-law model (with λ and bulk additions)

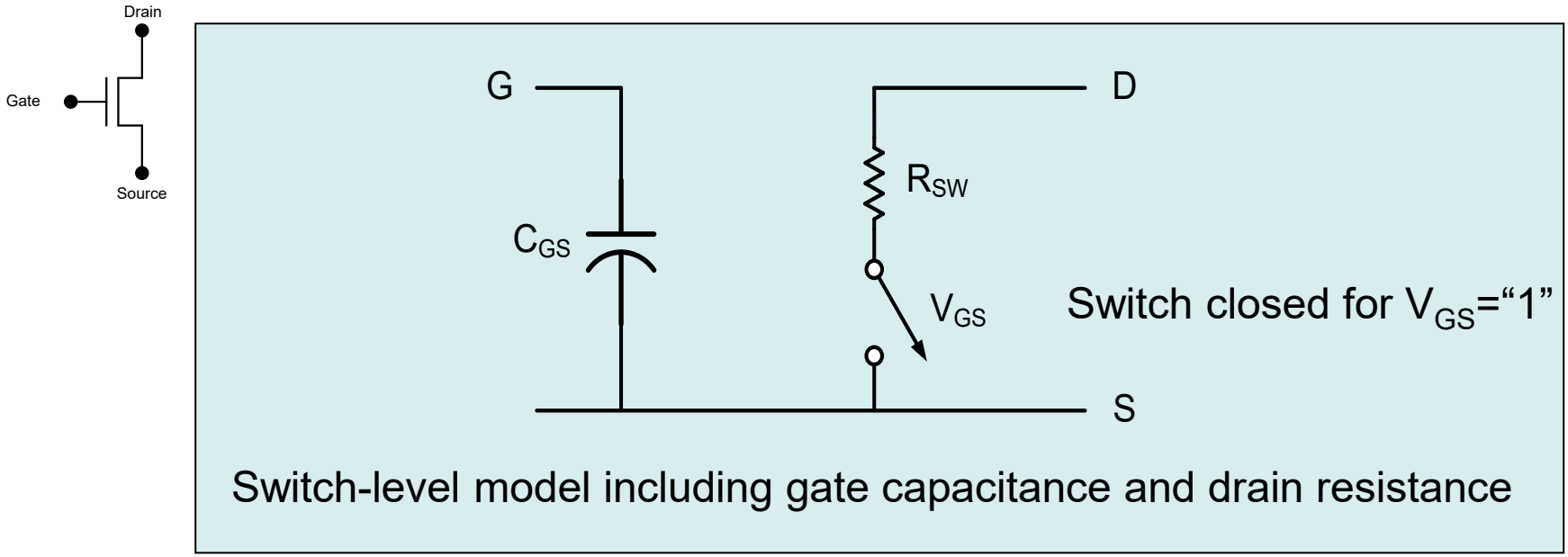
BSIM model

BSIM model (with binning extensions)

BSIM model (with binning extensions and process corners)

Review from last lecture

Switch-Level Models



Switch-level model including gate capacitance and drain resistance

C_{GS} and R_{SW} dependent upon device sizes and process

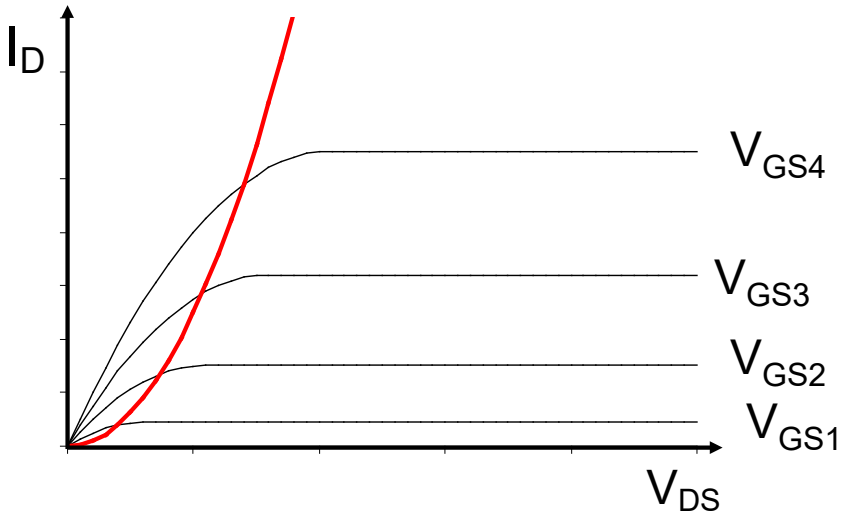
For minimum-sized devices in a 0.5u process

$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \left.\begin{array}{l} 2K\Omega \;\; n-channel \\ 6K\Omega \;\; p-channel \end{array}\right\}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Model Parameters : {C_{GS},R_{SW}}

Square-Law Model



$$I_D = \begin{cases} 0 & V_{GS} \le V_{TH} \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{TH} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_{TH} \quad V_{DS} < V_{GS} - V_{TH} \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{TH}\right)^2 & V_{GS} \ge V_{TH} \quad V_{DS} \ge V_{GS} - V_{TH} \end{cases}$$

Model Parameters : $\{\mu, C_{OX}, V_{TH0}\}$

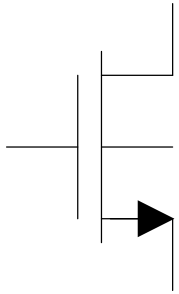
Design Parameters : $\{W,L\}$ but only one degree of freedom W/L

Review from last lecture

Extended Square-Law Model

$I_G = 0$

$I_B = 0$



$$I_D = \begin{cases} 0 & V_{GS} \le V_{TH} \\ \mu C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_{TH} \quad V_{DS} < V_{GS} - V_{TH} \\ \mu C_{OX} \frac{W}{2L}\left(V_{GS} - V_{TH}\right)^2 \bullet \left(1 + \lambda V_{DS}\right) & V_{GS} \ge V_{TH} \quad V_{DS} \ge V_{GS} - V_{TH} \end{cases}$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\varphi - V_{BS}} - \sqrt{\varphi}\right)$$

Model Parameters : $\{\mu, C_{OX}, V_{TH0}, \varphi, \gamma, \lambda\}$

Design Parameters : {W,L} but only one degree of freedom W/L

Review from last lecture

Short-Channel Model

$$I_D = \begin{cases} 0 & V_{GS} \le V_{TH} \\ \dfrac{\theta_2}{\theta_1}\mu C_{OX}\dfrac{W}{L}\left(V_{GS}-V_{TH}\right)^{\frac{\alpha}{2}}V_{DS} & V_{GS} \ge V_{TH} \quad V_{DS} < \theta_1\left(V_{GS}-V_{TH}\right)^{\frac{\alpha}{2}} \\ \theta_2\mu C_{OX}\dfrac{W}{L}\left(V_{GS}-V_{TH}\right)^{\alpha} & V_{GS} \ge V_{TH} \quad V_{DS} \ge \theta_1\left(V_{GS}-V_{TH}\right)^{\frac{\alpha}{2}} \end{cases}$$

α is the velocity saturation index, $2 \ge \alpha \ge 1$

Channel length modulation (λ) and bulk effects can be added to the velocity Saturation as well

Review from last lecture

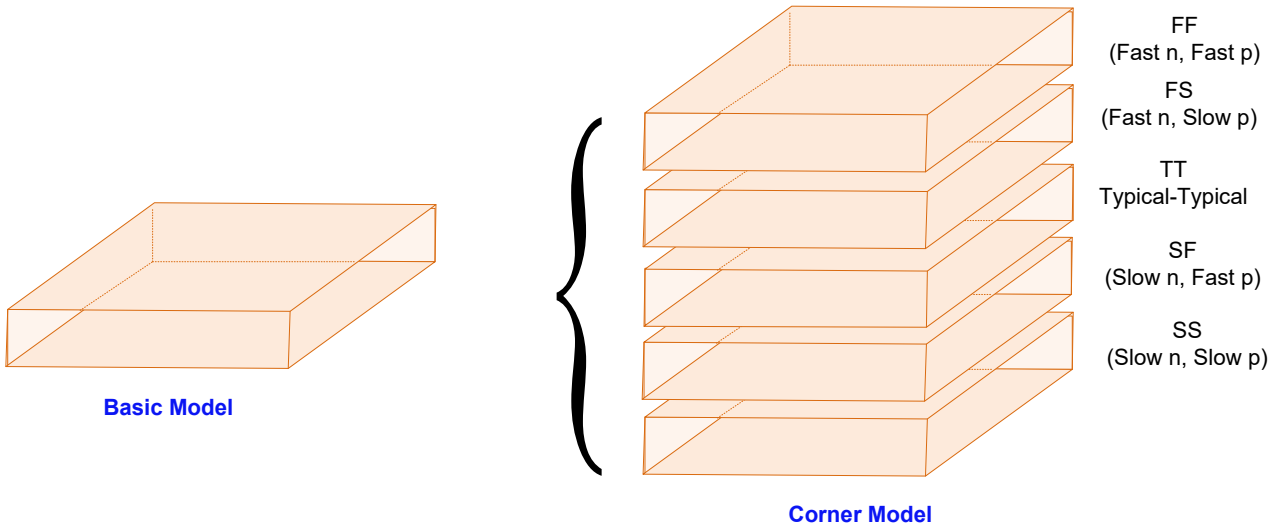
BSIM model

```
.MODEL CMOSN NMOS (
+VERSION = 3.1            TNOM    = 27              LEVEL   = 49
+XJ      = 1.5E-7         NCH     = 1.7E17          TOX     = 1.42E-8
+K1      = 0.8976376      K2      = -0.09255        VTH0    = 0.629035
+K3B     = -8.2369696     W0      = 1.041146E-8     K3      = 24.0984767
+DVT0W   = 0              DVT1W   = 0               NLX     = 1E-9
+DVT0    = 2.7123969      DVT1    = 0.4232931       DVT2W   = 0
+U0      = 451.2322004    UA      = 3.091785E-13    DVT2    = -0.1403765
+UC      = 1.22401E-11    VSAT    = 1.715884E5      UB      = 1.702517E-18
+AGS     = 0.130484       B0      = 2.446405E-6     A0      = 0.6580918
+KETA    = -3.043349E-3   A1      = 8.18159E-7      B1      = 5E-6
+RDSW    = 1.367055E3     PRWG    = 0.0328586       A2      = 0.3363058
+WR      = 1              WINT    = 2.443677E-7     PRWB    = 0.0104806
+XL      = 1E-7           XW      = 0               LINT    = 6.999776E-8
+DWB     = 3.676235E-8    VOFF    = -1.493503E-4    DWG     = -1.256454E-8
+CIT     = 0              CDSC    = 2.4E-4          NFACTOR = 1.0354201
+CDSCB   = 0              ETA0    = 2.342963E-3     CDSCD   = 0
+DSUB    = 0.0764123      PCLM    = 2.5941582       ETAB    = -1.5324E-4
+PDIBLC2 = 2.366707E-3    PDIBLCB = -0.0431505      PDIBLC1 = 0.8187825
+PSCBE1  = 6.611774E8     PSCBE2  = 3.238266E-4     DROUT   = 0.9919348
                                                   PVAG    = 0

+PRT     = 0              UTE     = -1.5            KT1     = -0.11
+KT1L    = 0              KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0              WLN     = 1               WW      = 0
+WWN     = 1              WWL     = 0               LL      = 0
+LLN     = 1              LW      = 0               LWN     = 1
+LWL     = 0              CAPMOD  = 2               XPART   = 0.5
+CGDO    = 2.32E-10       CGSO    = 2.32E-10        CGBO    = 1E-9
+CJ      = 4.282017E-4    PB      = 0.9317787       MJ      = 0.4495867
+CJSW    = 3.034055E-10   PBSW    = 0.8             MJSW    = 0.1713852
+CJSWG   = 1.64E-10       PBSWG   = 0.8             MJSWG   = 0.1713852
+CF      = 0              PVTH0   = 0.0520855       PRDSW   = 112.8875816
+PK2     = -0.0289036     WKETA   = -0.0237483      LKETA   = 1.728324E-3     )
*
```

Note this model has 95 model parameters !

Corner Models



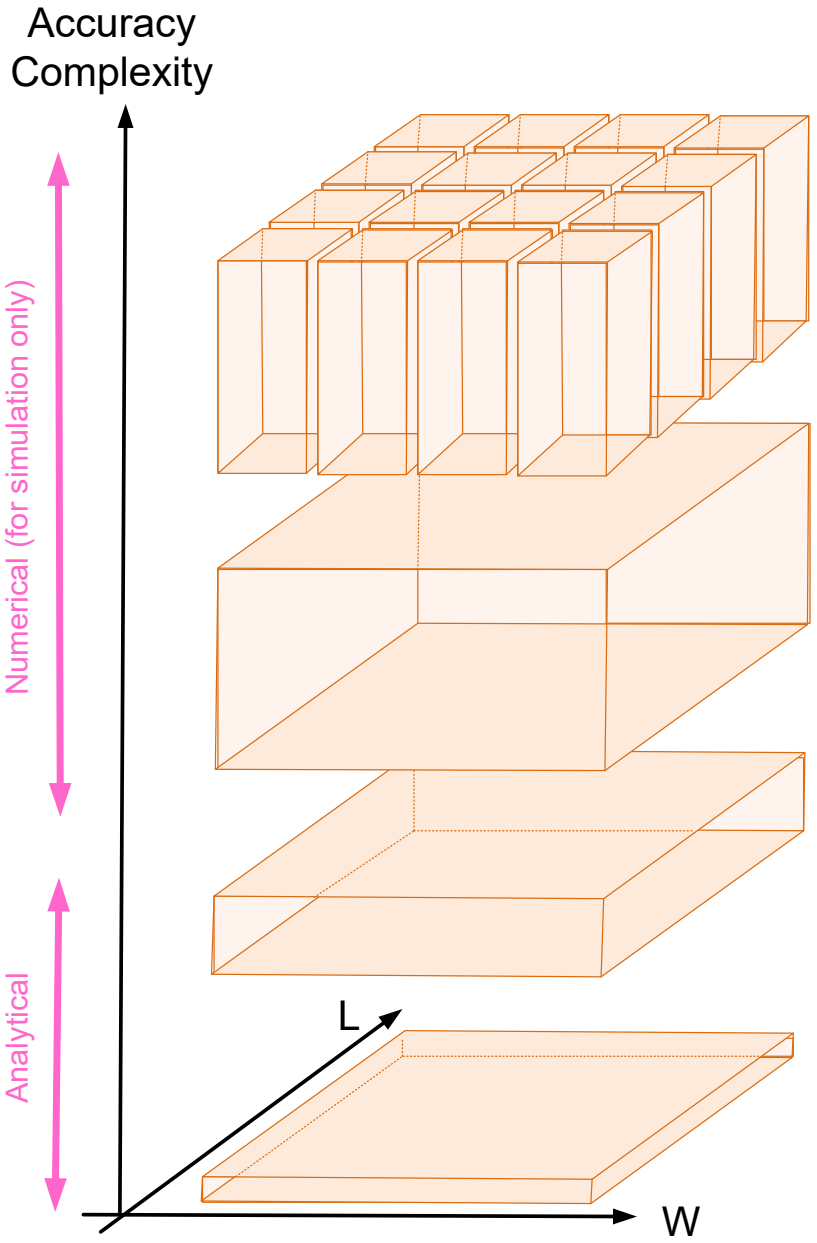
Applicable at any level in model hierarchy (same model, different parameters)

Often 4 corners (FF, FS, SF, SS) used but sometimes many more

Designers must provide enough robustness so good yield at all corners

Review from last lecture

Hierarchical Model Comparisons



BSIM Binning Models

Number of Model Parameters: **Approx 3000 (for 30 bins)**

BSIM Models

Number of Model Parameters: **Approx 100**

Square-Law Models

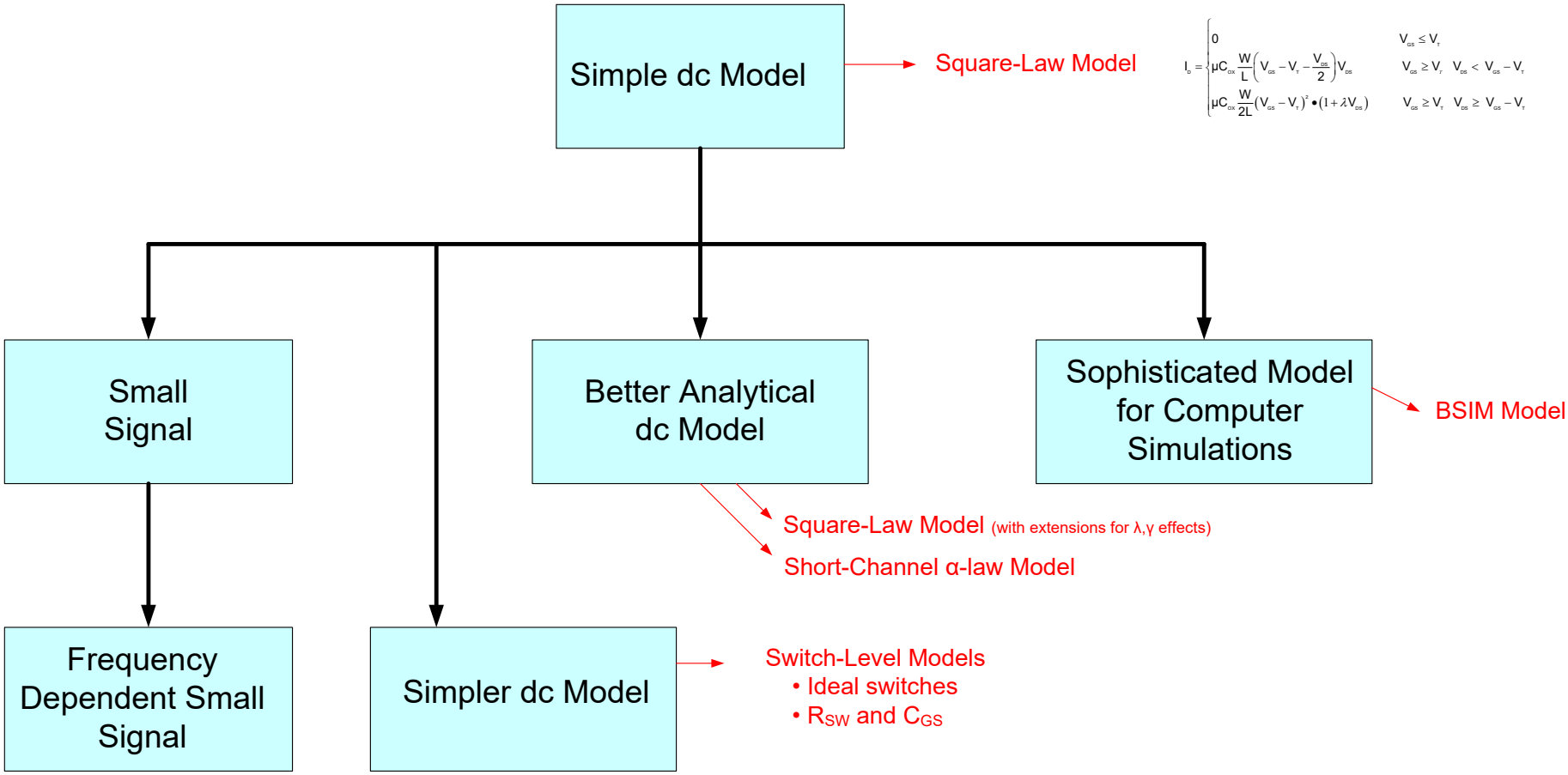
Number of Model Parameters: **3 to 6**

Switch-Level Models

Number of Model Parameters: **0 to 2**

Review from last lecture

Model Status

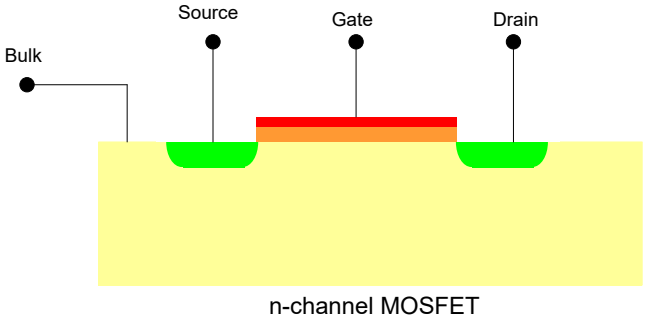


Relationship between N-channel and P-channel models

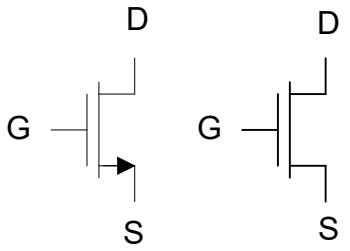
Basic models for n-channel and p-channel models are the same

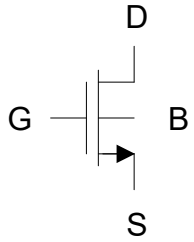
Major difference is in values for model parameters and direction of electrical port variables

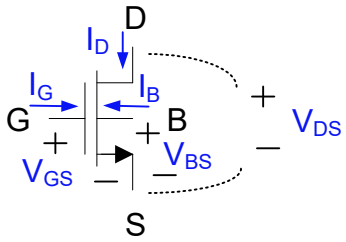
n-channel …. p-channel modeling

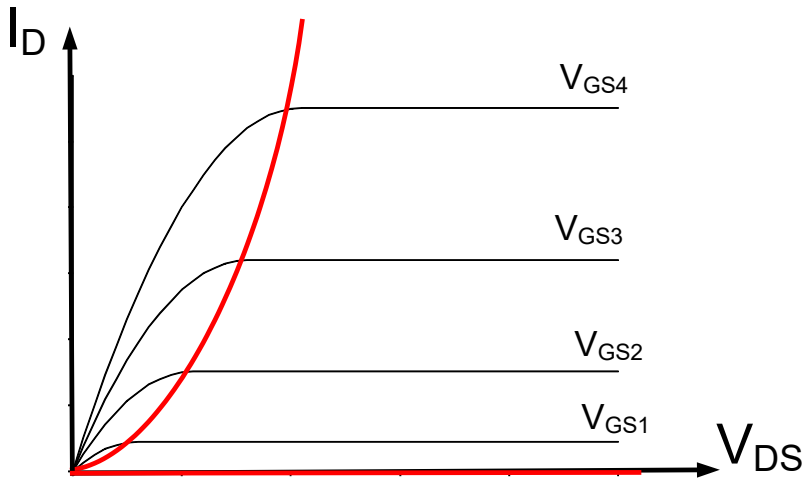


n-channel MOSFET









$V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > 0$

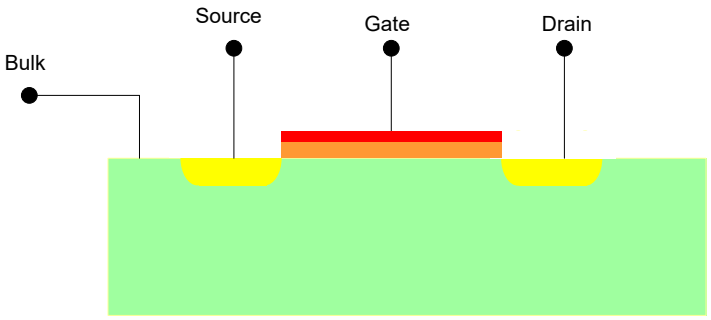
(for enhancement devices)

$$I_D = \begin{cases} 0 & V_{GS} \le V_{Tn} \\ \mu_n C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tn} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_{Tn} \quad V_{DS} < V_{GS} - V_{Tn} \\ \mu_n C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tn}\right)^2 & V_{GS} \ge V_{Tn} \quad V_{DS} \ge V_{GS} - V_{Tn} \end{cases}$$

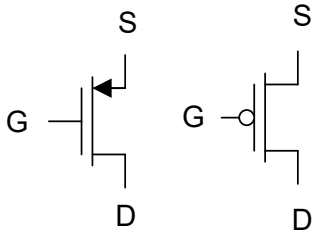
$I_G = I_B = 0$

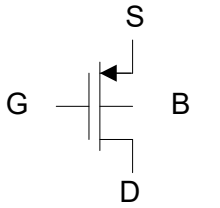
Positive V_{DS} and V_{GS} cause a positive I_D

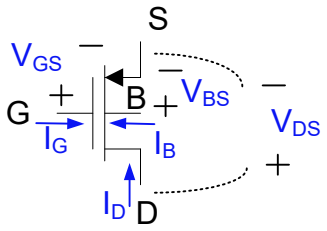
n-channel …. p-channel modeling



p-channel MOSFET

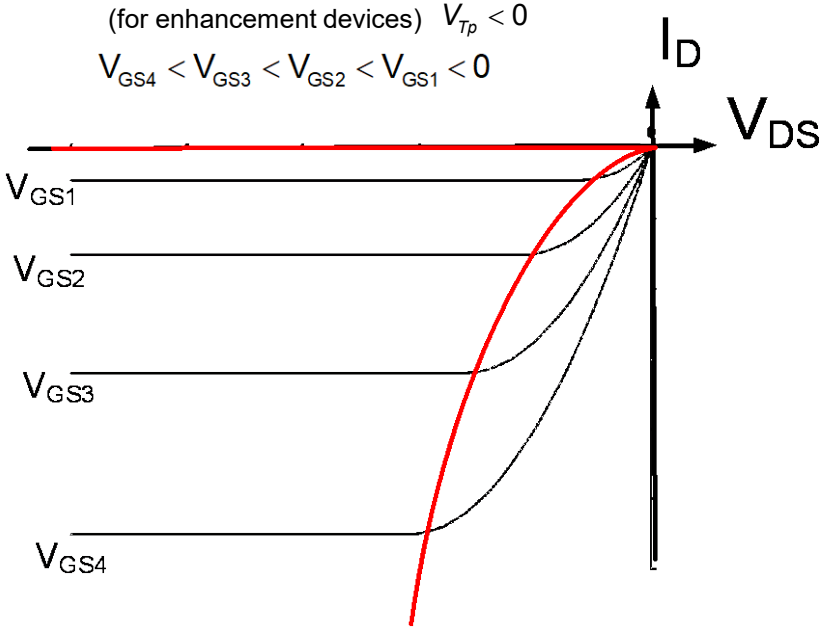






(for enhancement devices) $V_{Tp} < 0$

$V_{GS4} < V_{GS3} < V_{GS2} < V_{GS1} < 0$



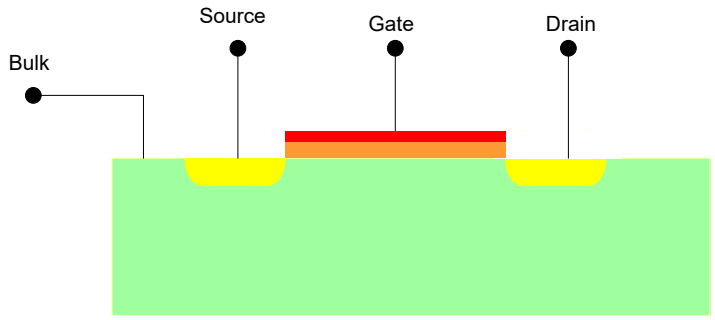
$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \frac{W}{L}\left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \frac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$I_G = I_B = 0$

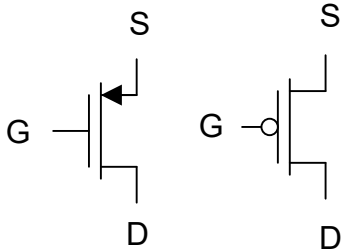
Negative V_{DS} and V_{GS} cause a negative I_D

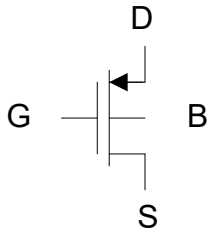
Functional form of models are the same, just sign differences and some parameter differences (usually mobility is the most important)

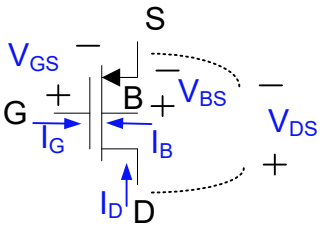
n-channel …. p-channel modeling

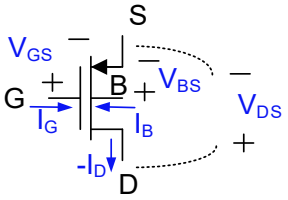


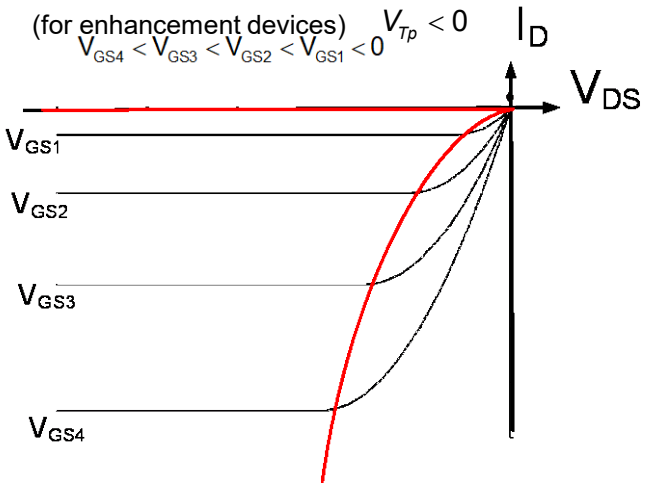
p-channel MOSFET









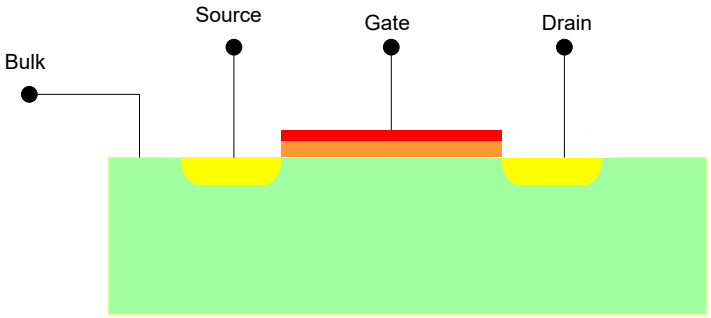


$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \frac{W}{L}\left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \frac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

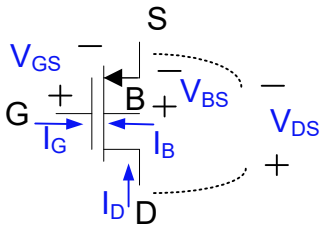
$$I_G = I_B = 0$$

- Actually should use C_{OXp} and C_{OXn} but they are usually almost identical in most processes
- $\mu_n \approx 3\mu_p$
- May choose to model $-I_D$ which will be non-negative

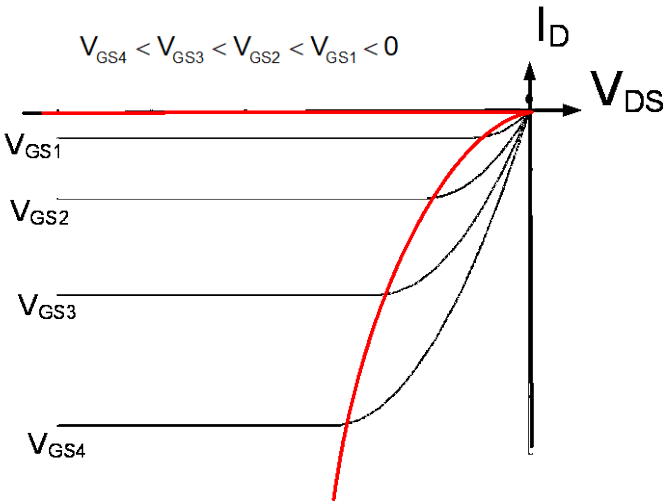
n-channel …. p-channel modeling



p-channel MOSFET



(for enhancement devices)



$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \frac{W}{L}\left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \frac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$I_G = I_B = 0$

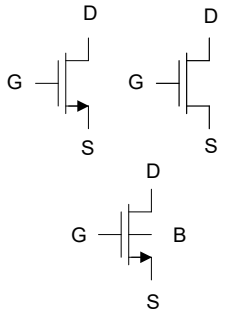
Alternate equivalent representation w/o sign convention

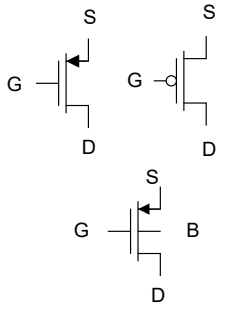
$$|I_D| = \begin{cases} 0 & |V_{GS}| \leq |V_{Tp}| \\ \mu_p C_{OX} \frac{W}{L}\left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2}\right)V_{DS} & |V_{GS}| \geq |V_{Tp}| \quad |V_{DS}| < |V_{GS} - V_{Tp}| \\ \mu_p C_{OX} \frac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & |V_{GS}| \geq |V_{Tp}| \quad |V_{DS}| \geq |V_{GS} - V_{Tp}| \end{cases}$$

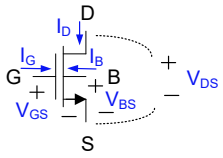
$I_G = I_B = 0$

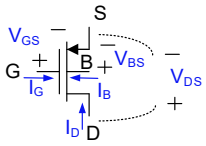
These look like those for the n-channel device but with | |

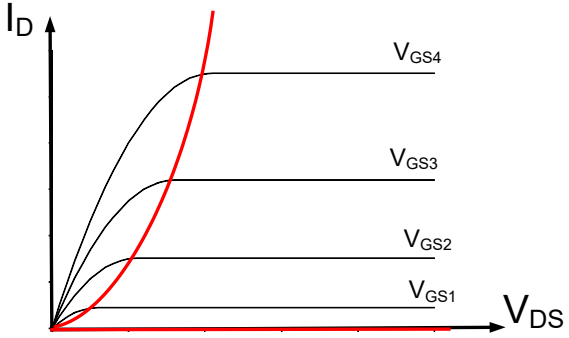
n-channel …. p-channel modeling





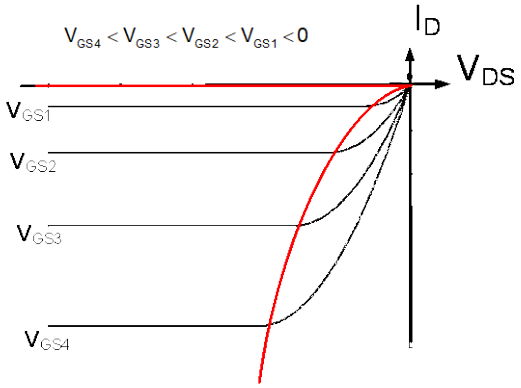






$V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > 0$

Models essentially the same with different signs and model parameters



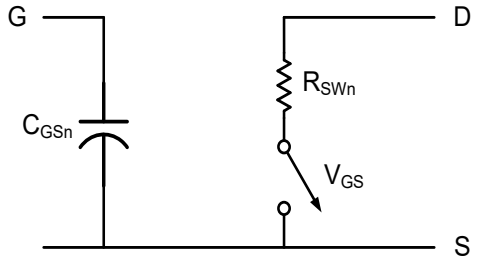
$$I_D = \begin{cases} 0 & V_{GS} \le V_{Tn} \\ \mu_n C_{OX} \frac{W}{L}\left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_{Tn} \quad V_{DS} < V_{GS} - V_{Tn} \\ \mu_n C_{OX} \frac{W}{2L}\left(V_{GS} - V_{Tn}\right)^2 & V_{GS} \ge V_{Tn} \quad V_{DS} \ge V_{GS} - V_{Tn} \end{cases}$$

$I_G = I_B = 0$

$$I_D = \begin{cases} 0 & V_{GS} \ge V_{Tp} \\ -\mu_p C_{OX} \frac{W}{L}\left(V_{GS} - V_{Tp} - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \le V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \frac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \le V_{Tp} \quad V_{DS} \le V_{GS} - V_{Tp} \end{cases}$$

$I_G = I_B = 0$

Model Relationships



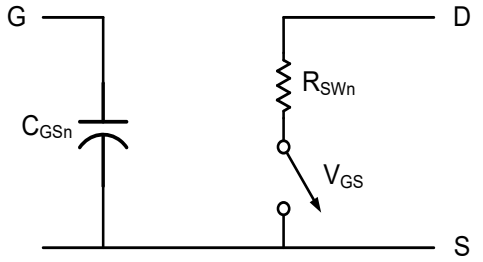
Determine R_{SW} and C_{GS} in the switch-level model for an n-channel MOSFET from square-law model in a CMOS process if L=1u, W=1u

(Assume $\mu_n C_{OX}=100\mu AV^{-2}$, $C_{OX}=2.5fFu^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \mu C_{OX}\dfrac{W}{L}\left(V_{GS}-V_T-\dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS}-V_T \\ \mu C_{OX}\dfrac{W}{2L}\left(V_{GS}-V_T\right)^2 & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS}-V_T \end{cases}$$

when SW is on, operation is “deep” triode

Model Relationships



Determine R_{SW} and C_{GS} for an n-channel MOSFET from square-law model in a CMOS process if L=1u, W=1u

(Assume $\mu_n C_{OX}=100\mu AV^{-2}$, $C_{OX}=2.5fFu^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

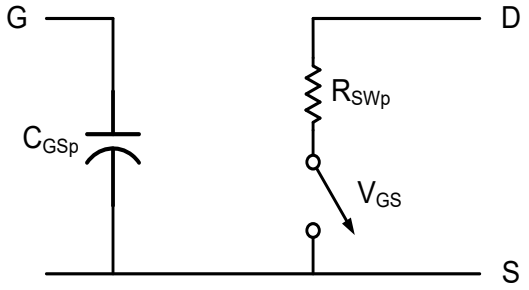
When on operating in deep triode

$$I_D = \mu C_{OX}\frac{W}{L}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)V_{DS} \cong \mu C_{OX}\frac{W}{L}\left(V_{GS}-V_T\right)V_{DS}$$

$$R_{SQ} = \left.\frac{V_{DS}}{I_D}\right|_{V_{GS}=V_{DD}} = \left.\frac{1}{\mu C_{OX}\frac{W}{L}\left(V_{GS}-V_T\right)}\right|_{V_{GS}=3.5V} = \frac{1}{(10^{-4})\left(\frac{1}{1}\right)(3.5-1)} = 4K\Omega$$

$C_{GS}= C_{OX}WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF$

Model Relationships



Determine R_{SW} and C_{GS} for an p-channel MOSFET from square-law model in the 0.5u ON CMOS process if L=1u, W=1u

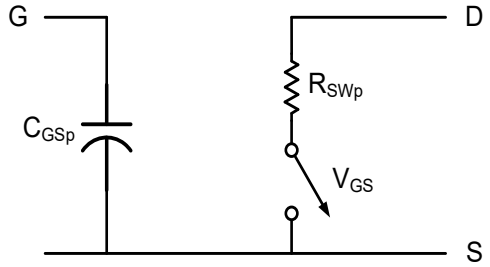
($\mu_p C_{OX}$=33μAV^{-2} , $\mu_n C_{OX}$=100μAV^{-2} , C_{OX}=2.5fFu^{-2},V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0)

Observe $\mu_n \backslash \mu_p \approx 3$

$$-I_D = \begin{cases} 0 & V_{GS} \geq V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_T \quad V_{DS} > V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 & V_{GS} \leq V_T \quad V_{DS} \leq V_{GS} - V_T \end{cases}$$

When SW is on, operation is “deep” triode

Model Relationships



Determine R_{SW} and C_{GS} for an p-channel MOSFET from square-law model in a CMOS process if L=1u, W=1u

($\mu_p C_{OX} = \frac{1}{3}\mu_n C_{OX}$, $\mu_n C_{OX}=100\mu AV^{-2}$, $C_{OX}=2.5fFu^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

$$-I_D = \mu_p C_{OX}\frac{W}{L}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)V_{DS} \cong \mu_p C_{OX}\frac{W}{L}\left(V_{GS}-V_T\right)V_{DS}$$

$$R_{SQ} = \left.\frac{-V_{DS}}{-I_D}\right|_{V_{GS}=V_{DD}} = \left.\frac{1}{\mu_p C_{OX}\frac{W}{L}\left(V_{GS}-V_T\right)}\right|_{V_{GS}=3.5V} = \frac{1}{\left(\left(\frac{1}{3}\right)10^{-4}\right)\left(\frac{1}{1}\right)\left|3.5-1\right|} = 12K\Omega$$

$C_{GS} = C_{OX}WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF$

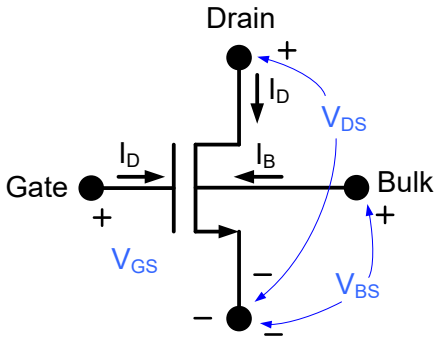
Observe the resistance of the p-channel device is approximately 3 times larger than that of the n-channel device for same bias and dimensions !

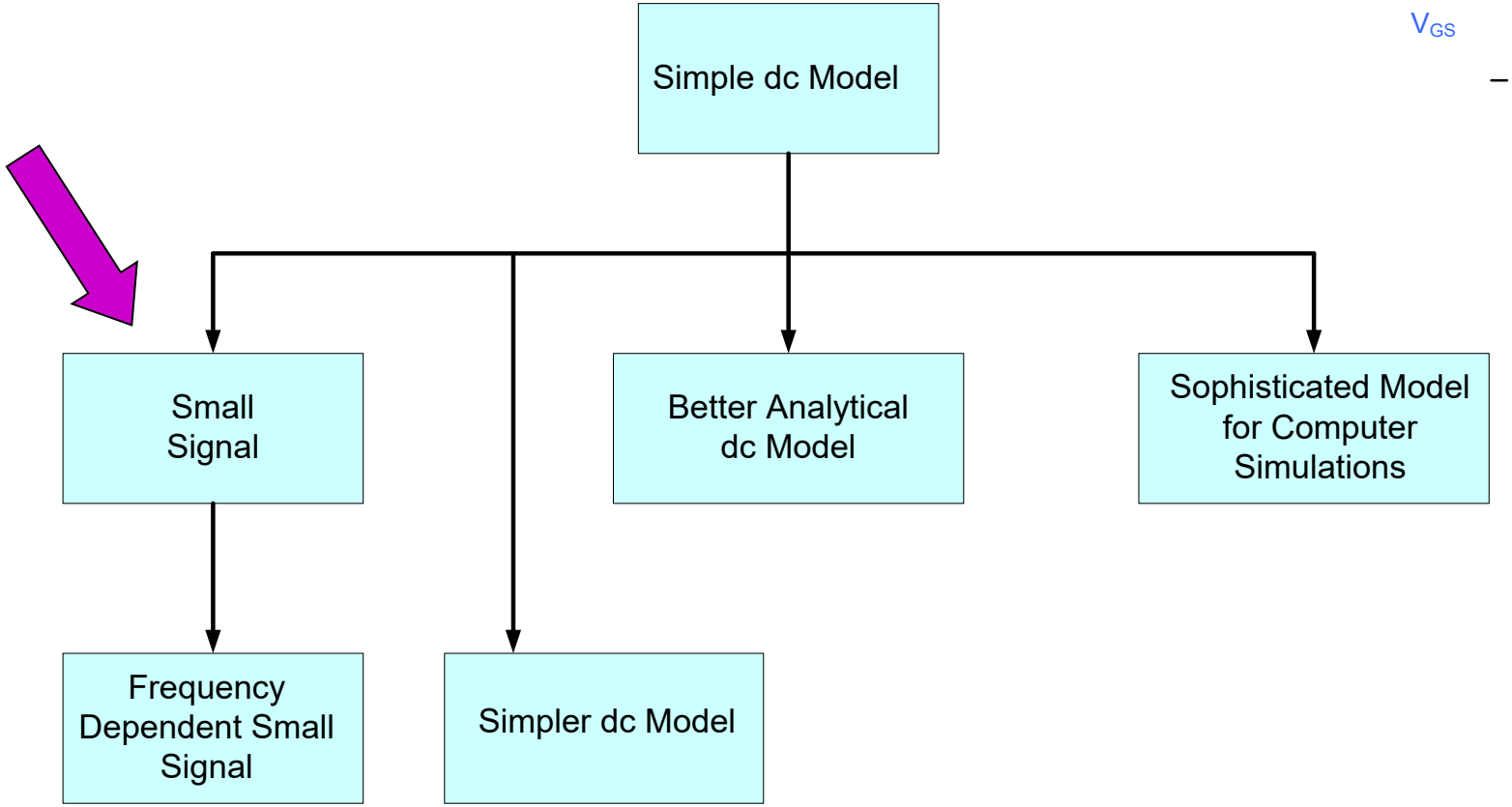
This is due to the difference in mobility between n-type and p-type materials

Modeling of the MOSFET

Goal: Obtain a mathematical relationship between the port variables of a device.

$$I_D = f_1(V_{GS}, V_{DS}, V_{BS})$$
$$I_G = f_2(V_{GS}, V_{DS}, V_{BS})$$
$$I_B = f_3(V_{GS}, V_{DS}, V_{BS})$$



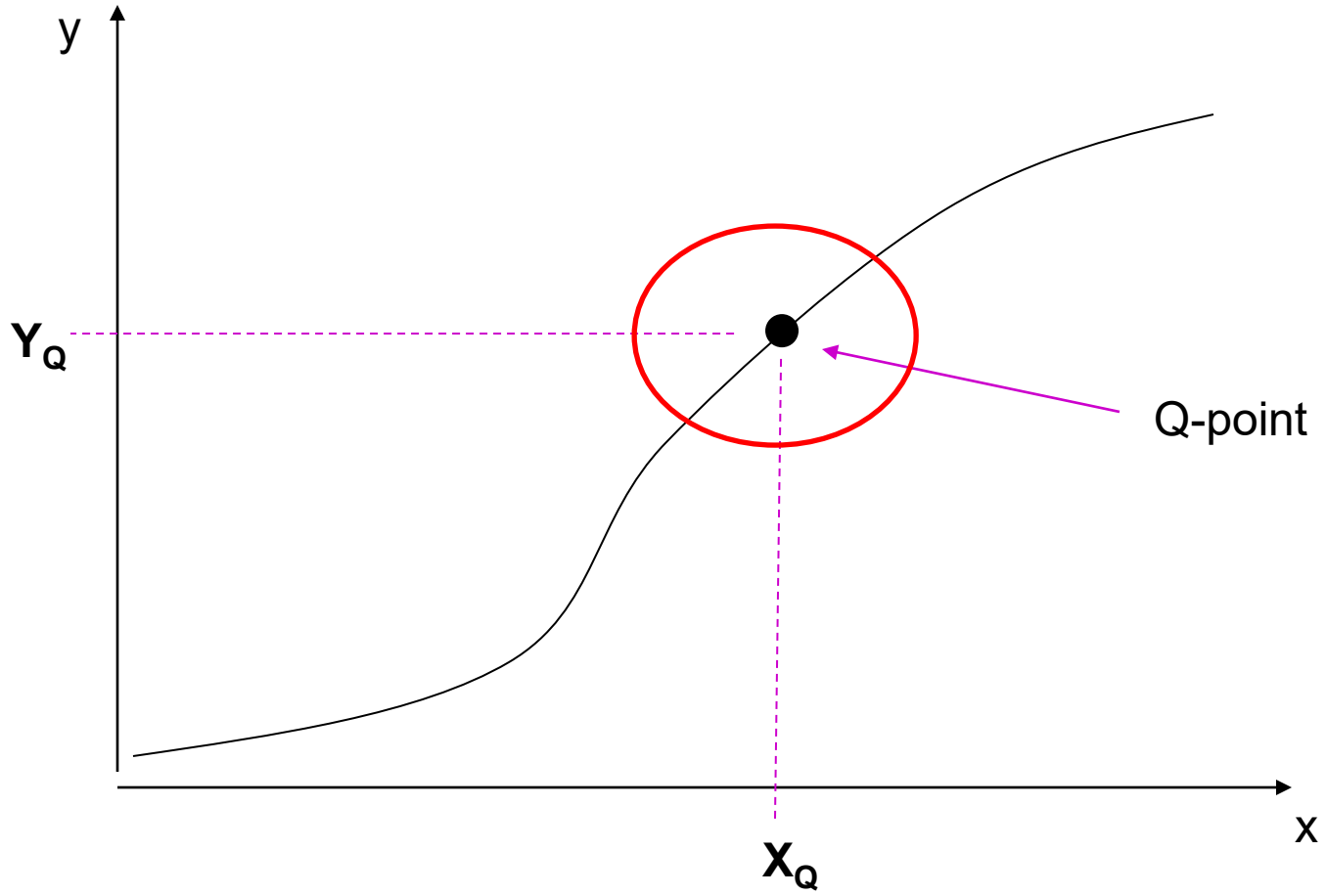


Small-Signal Model

Goal with small signal model is to predict performance of circuit or device in the vicinity of an operating point

Operating point is often termed Q-point

Small-Signal Model



- **Behaves linearly in the vicinity of the Q-point**
- **Analytical expressions for small signal model will be developed later**

Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT

Lets pick up a discussion of another part of the Technology Files before moving to BJT

Technology Files

- Design Rules
- Process Flow (Fabrication Technology)
- Model Parameters

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN **n-well**	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus **n**-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT **p**-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25. Strip photoresist
Optional steps for double polysilicon process
B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist

43.	APPLY METAL	
44.	Apply photoresist	
45.	PATTERN METAL	(MASK #7)
46.	Develop photoresist	
47.	Etch metal	
48.	Strip photoresist	
	Optional steps for double metal process	
	C.1 Strip thin oxide	
	C.2 DEPOSIT INTERMETAL OXIDE	
	C.3 Apply photoresist	
	C.4 PATTERN VIAS	(MASK #C1)
	C.5 Develop photoresist	
	C.6 Etch oxide	
	C.7 Strip photoresist	
	C.8 APPLY METAL (Metal 2)	
	C.9 Apply photoresist	
	C.10 PATTERN METAL	(MASK #C2)
	C.11 Develop photoresist	
	C.12 Etch metal	
	C.13 Strip photoresist	
49.	APPLY PASSIVATION	
50.	Apply photoresist	
51.	PATTERN PAD OPENINGS	(MASK #8)
52.	Develop photoresist	
53.	Etch passivation	
54.	Strip photoresist	
55.	ASSEMBLE, PACKAGE AND TEST	

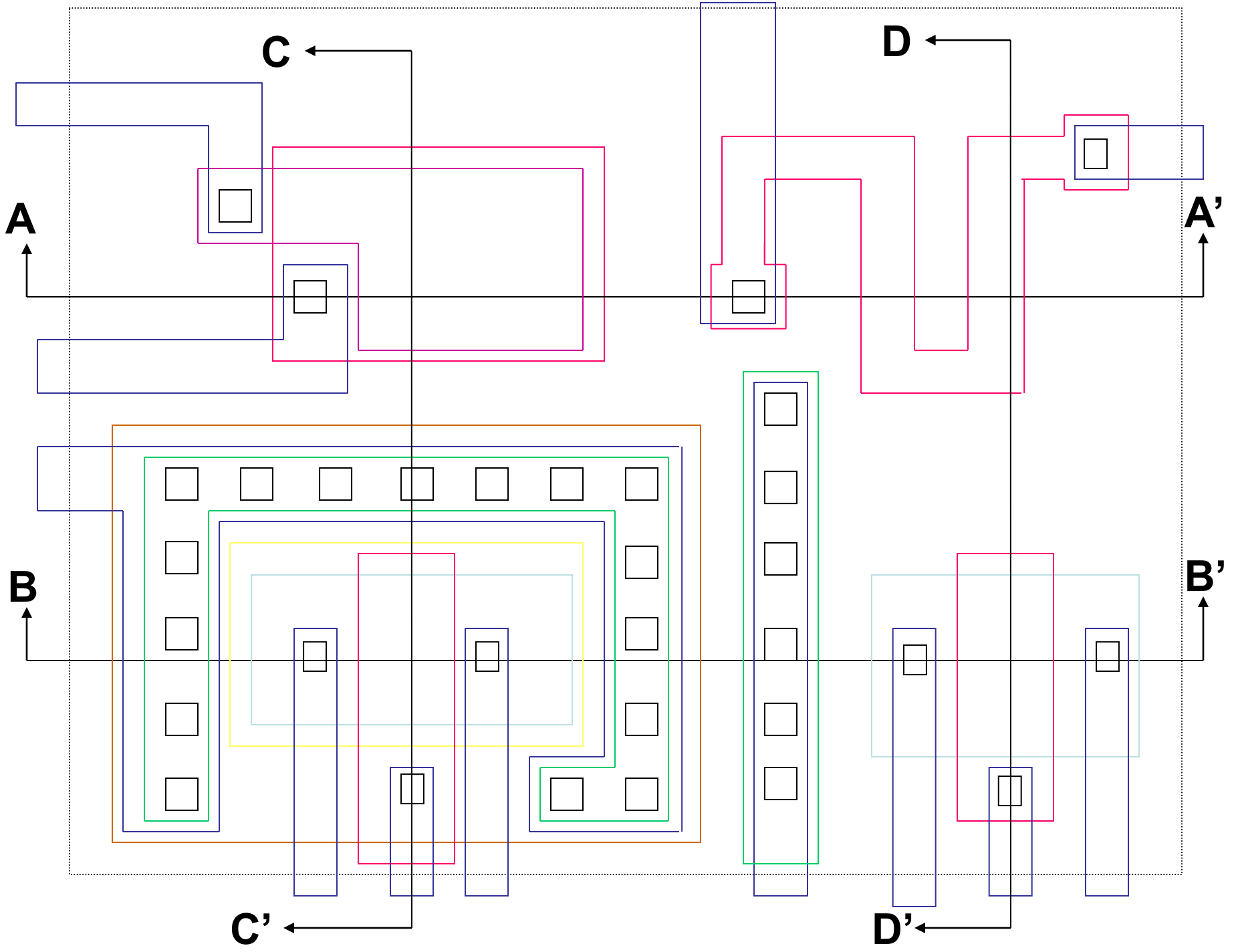
Bulk CMOS Process Description

- n-well process
- Single Metal Only Depicted
- Double Poly

- This type of process dominates what is used for high-volume “low-cost” processing of integrated circuits today
- Many process variants and specialized processes are used for lower-volume or niche applications
- Emphasis in this course will be on the electronics associated with the design of integrated electronic circuits in processes targeting high-volume low-cost products where competition based upon price differentiation may be acute
- Basic electronics concepts, however, are applicable for lower-volume or niche applicaitons

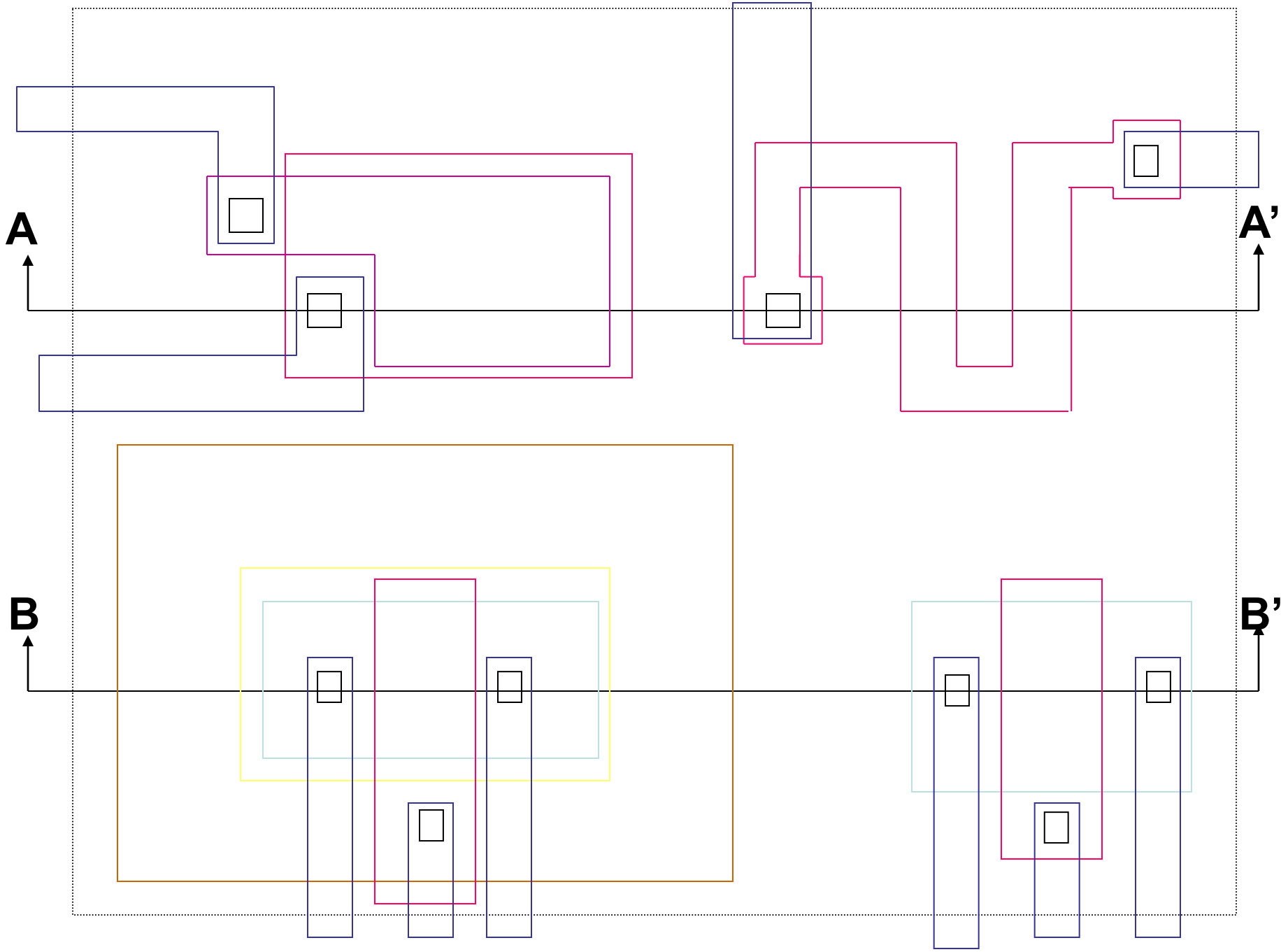
Components Shown

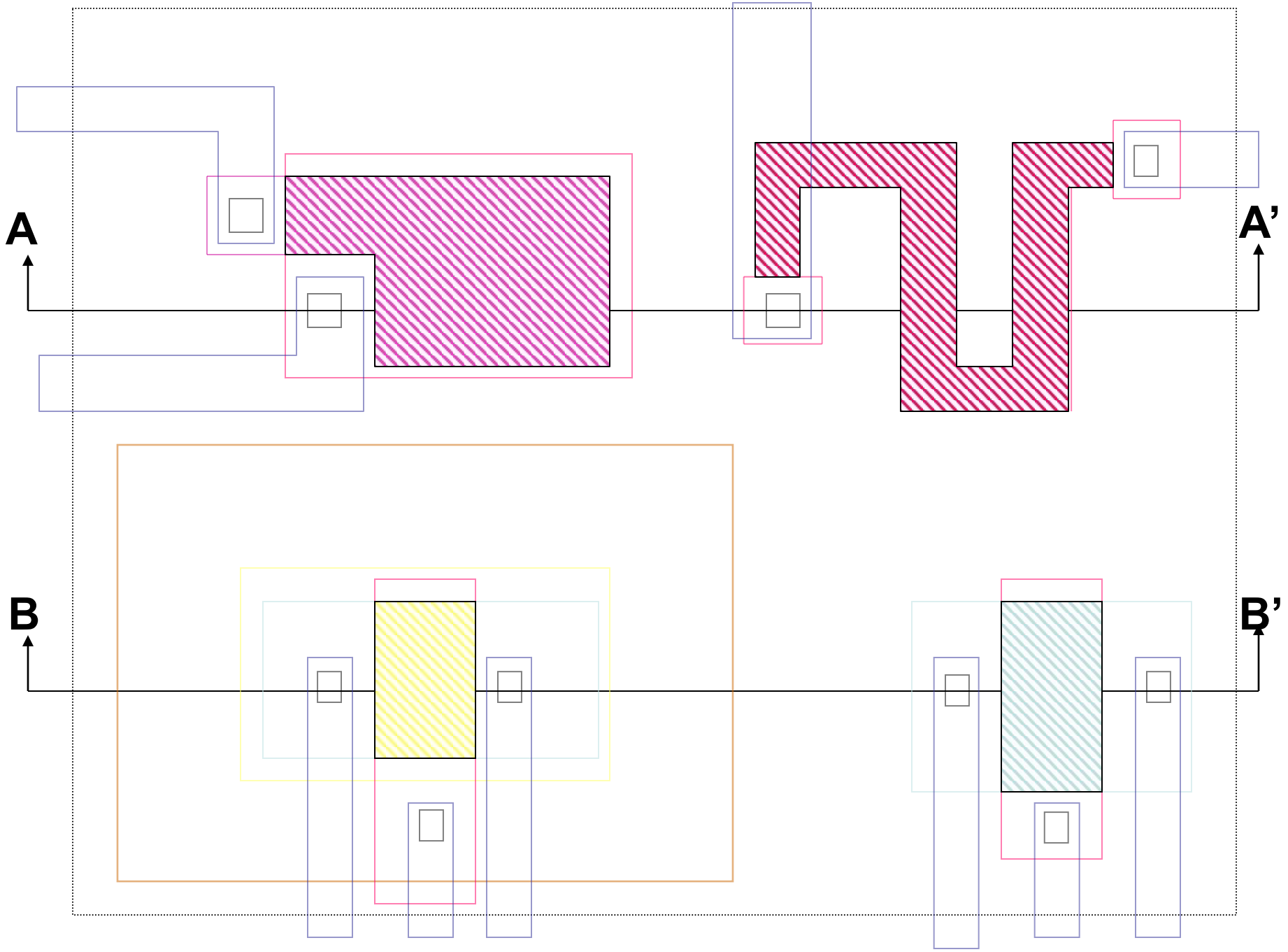
- n-channel MOSFET
- p-channel MOSFET
- Poly Resistor
- Doubly Poly Capacitor

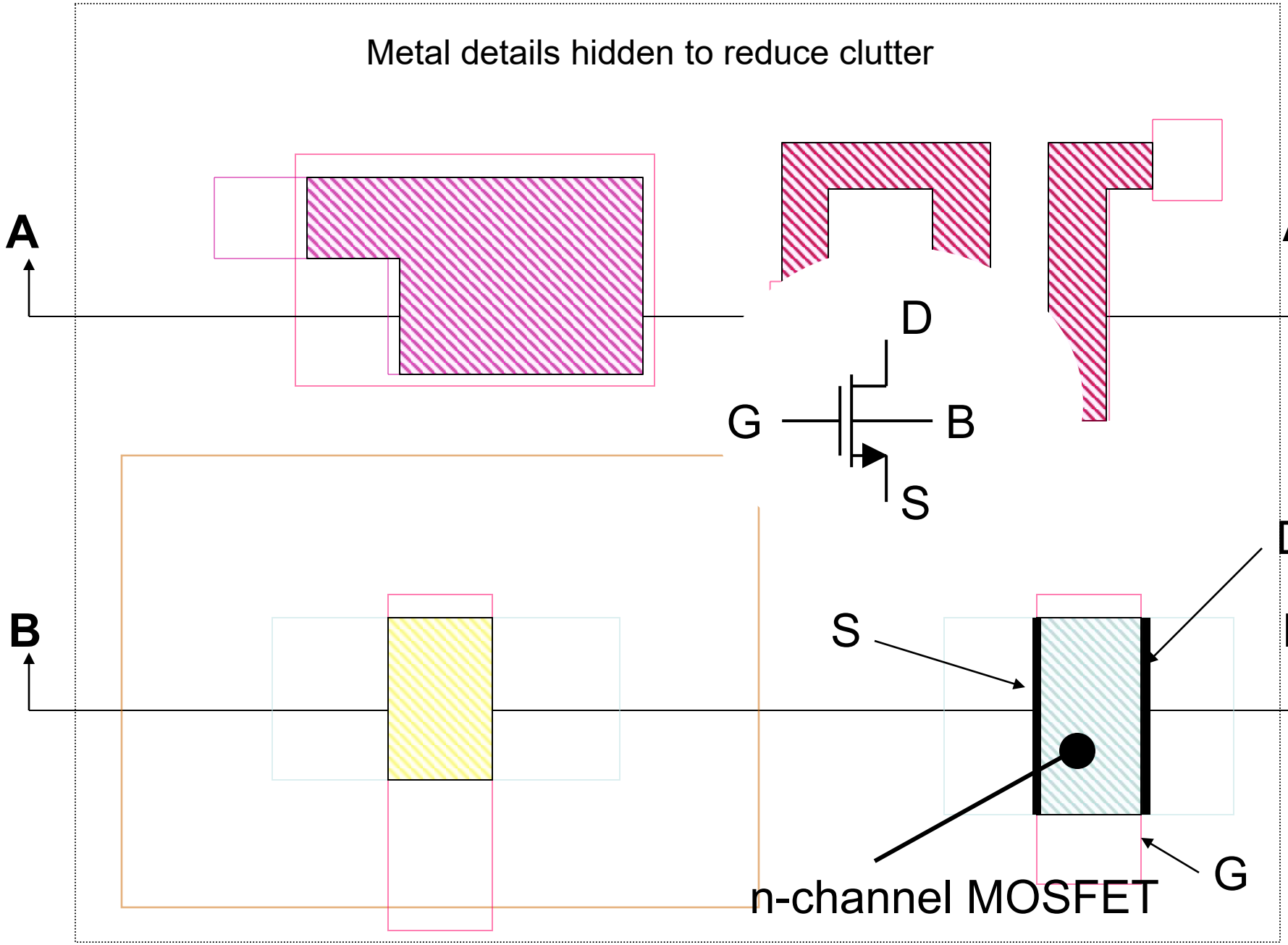

C
D
A
A’
B
B’
C’
D’

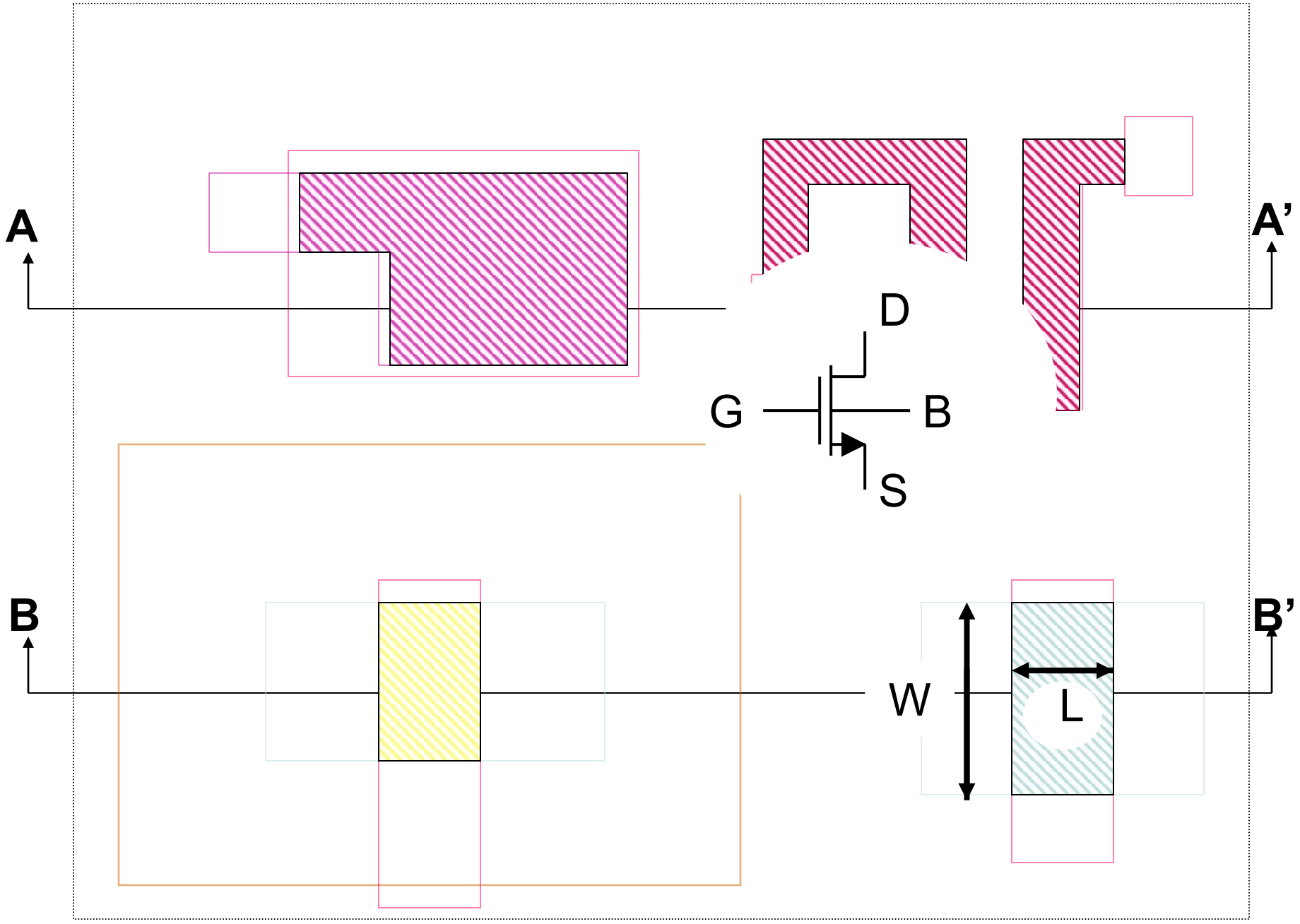
Consider Basic Components Only

Well Contacts and Guard Rings Will be Discussed Later


A
A’
B
B’


A
A'
B
B'


Metal details hidden to reduce clutter
A
A'
D
G
B
S
B
B'
S
D
G
n-channel MOSFET


A
A'
D
G
B
S
B
B'
W
L

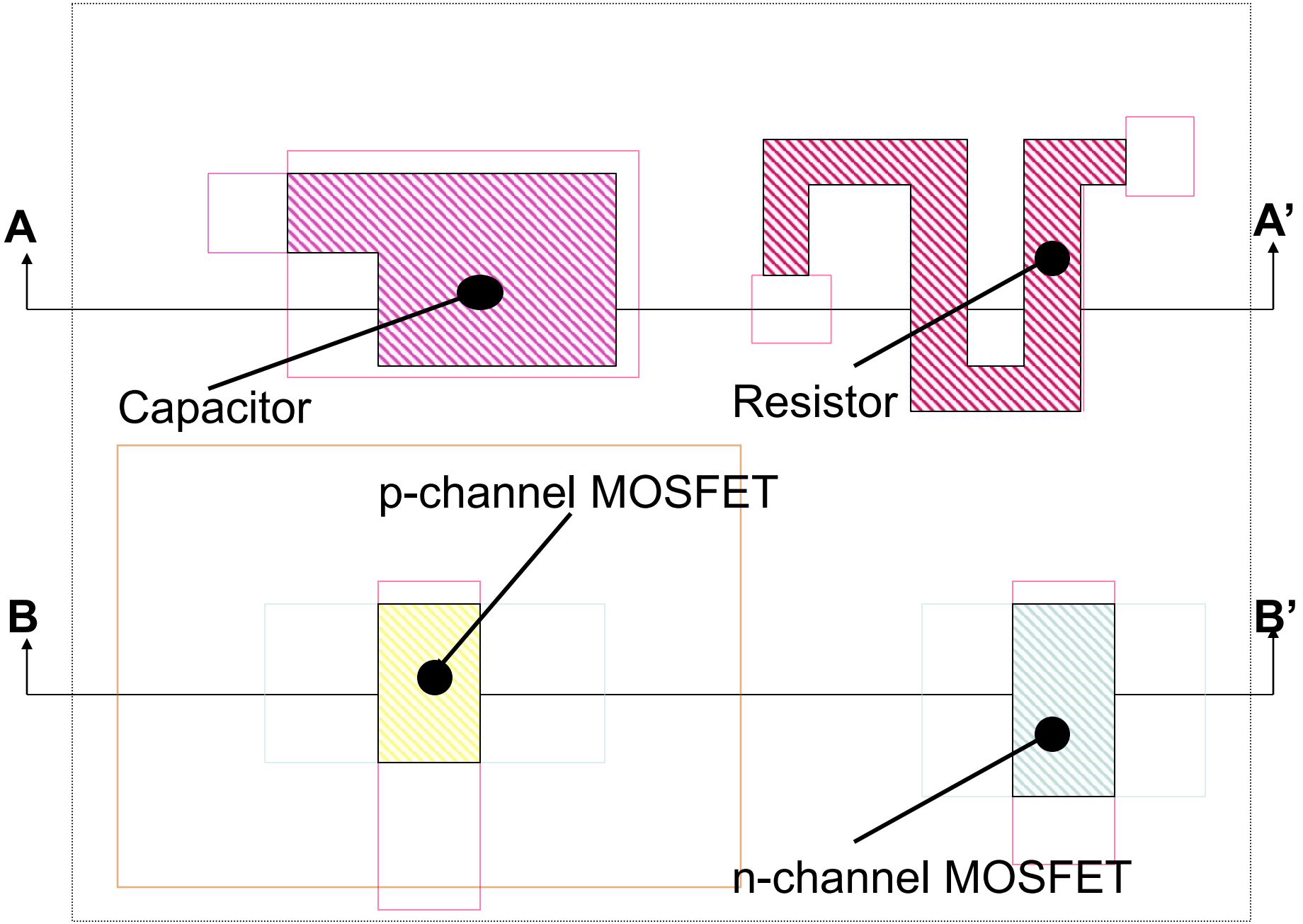
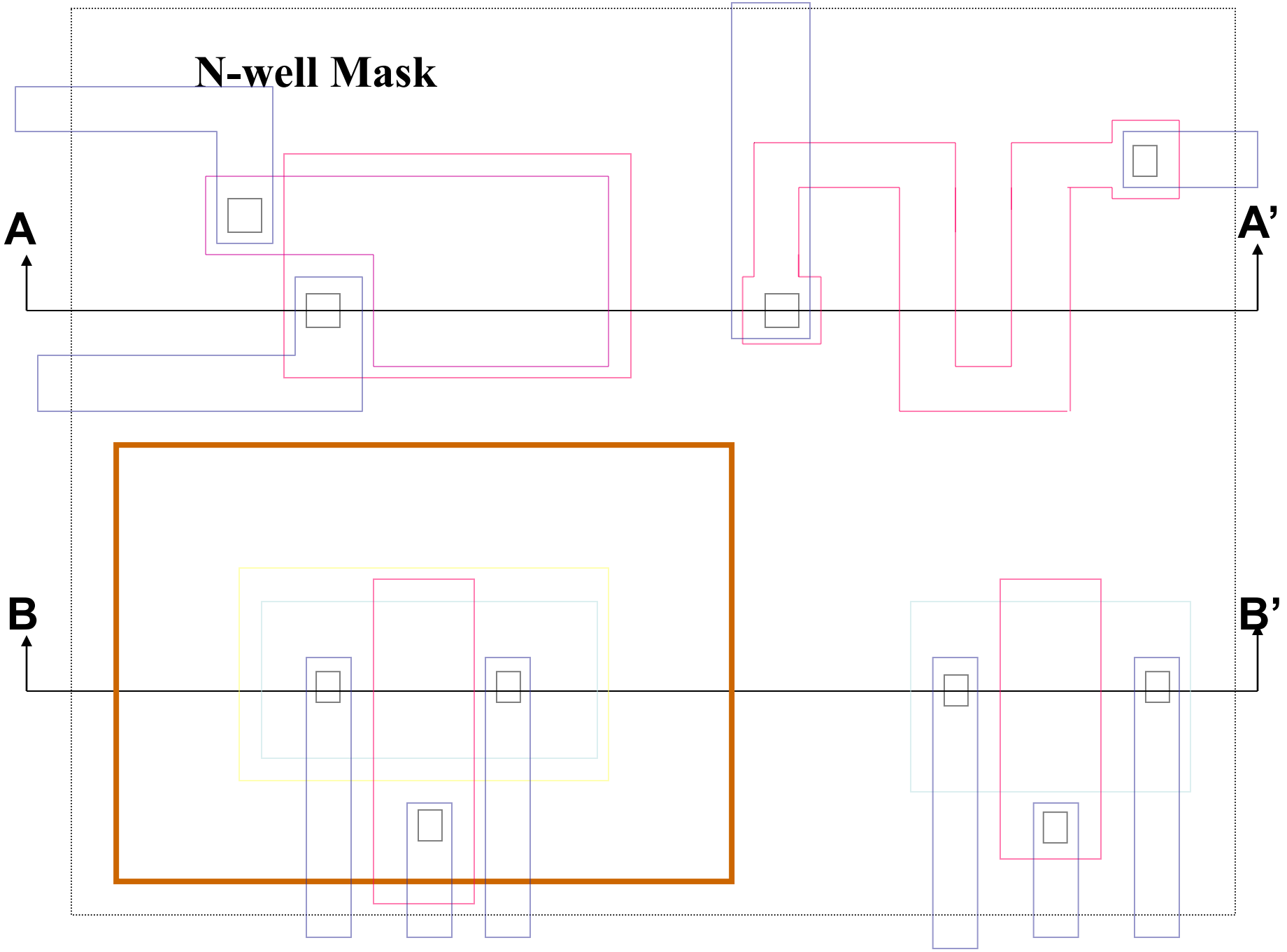
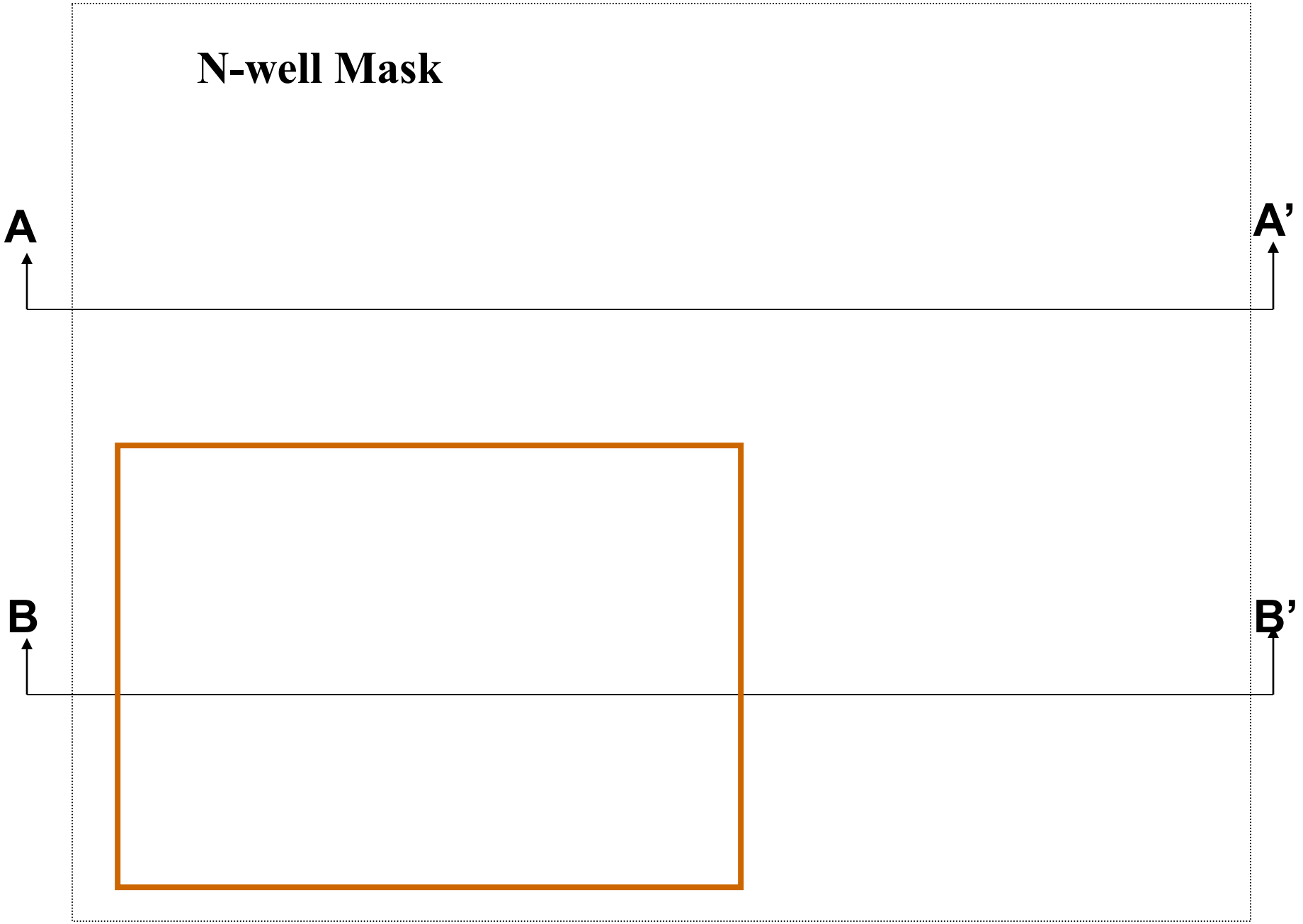

A
A'
Capacitor
Resistor
p-channel MOSFET
B
B'
n-channel MOSFET

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN **n-well**	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus **n**-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT **p**-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

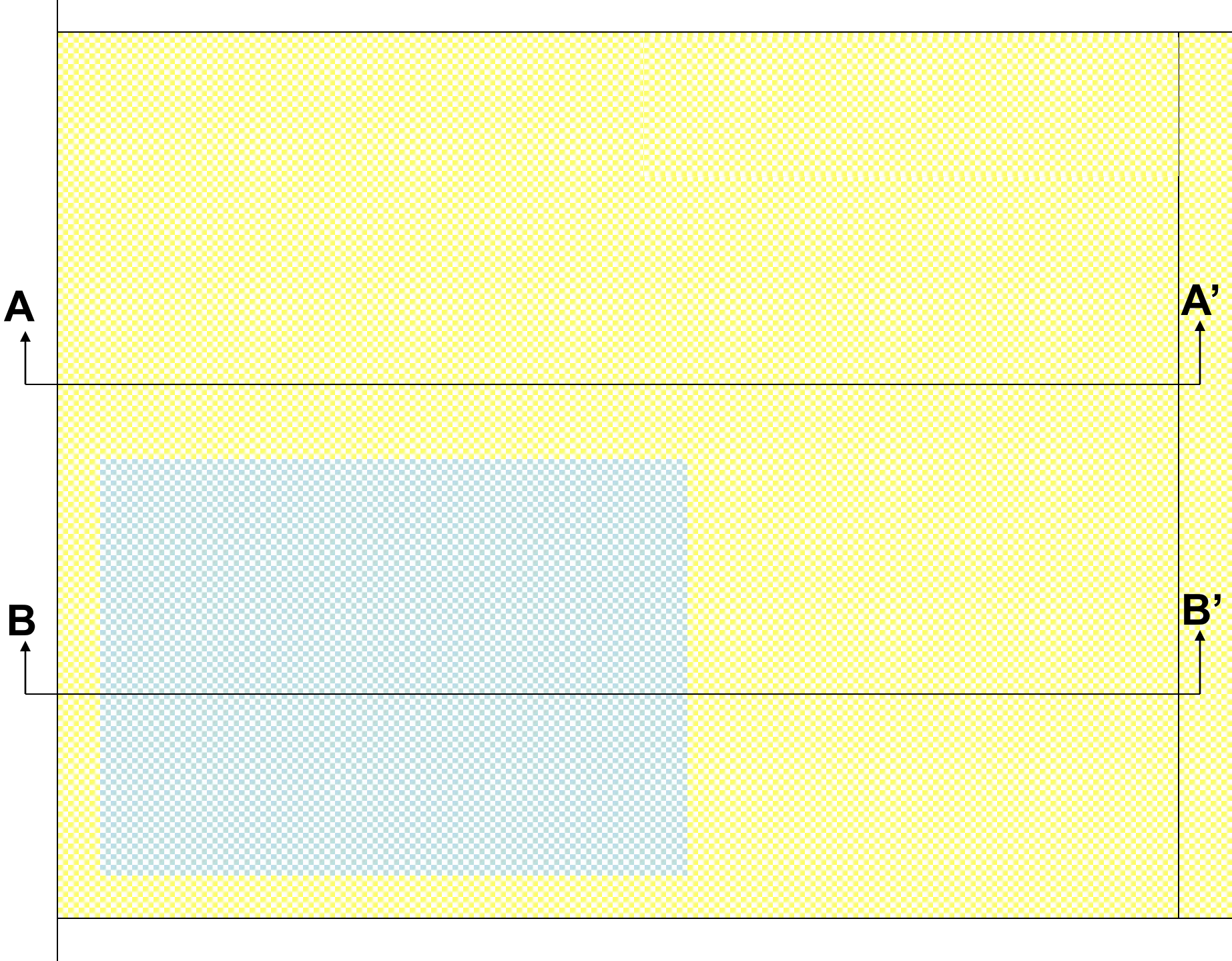
n-well mask


N-well Mask
A
A’
B
B’


N-well Mask
A
A’
B
B’

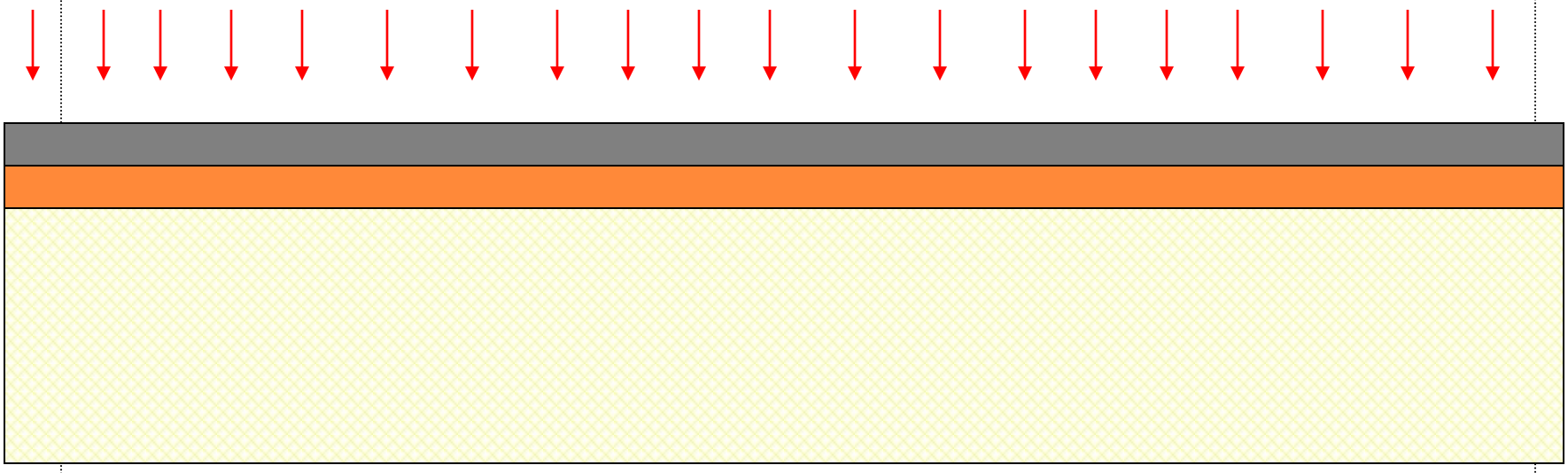
Detailed Description of First Photolithographic Steps Only

- Top View
- Cross-Section View

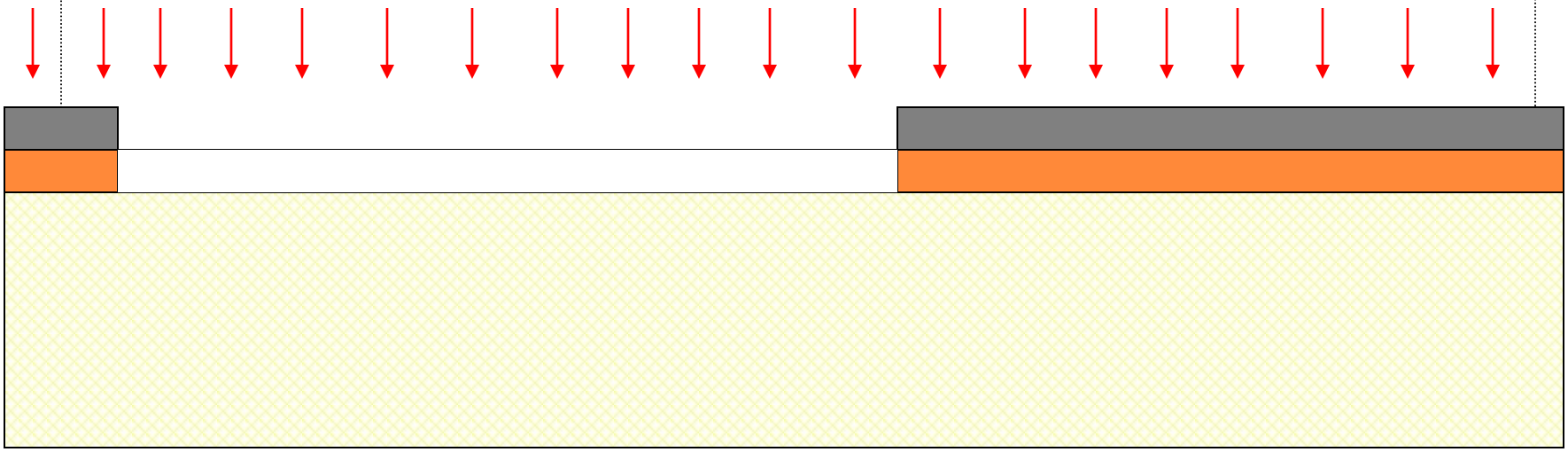

A
A’
B
B’

Shown as mask but actually projection through reticle

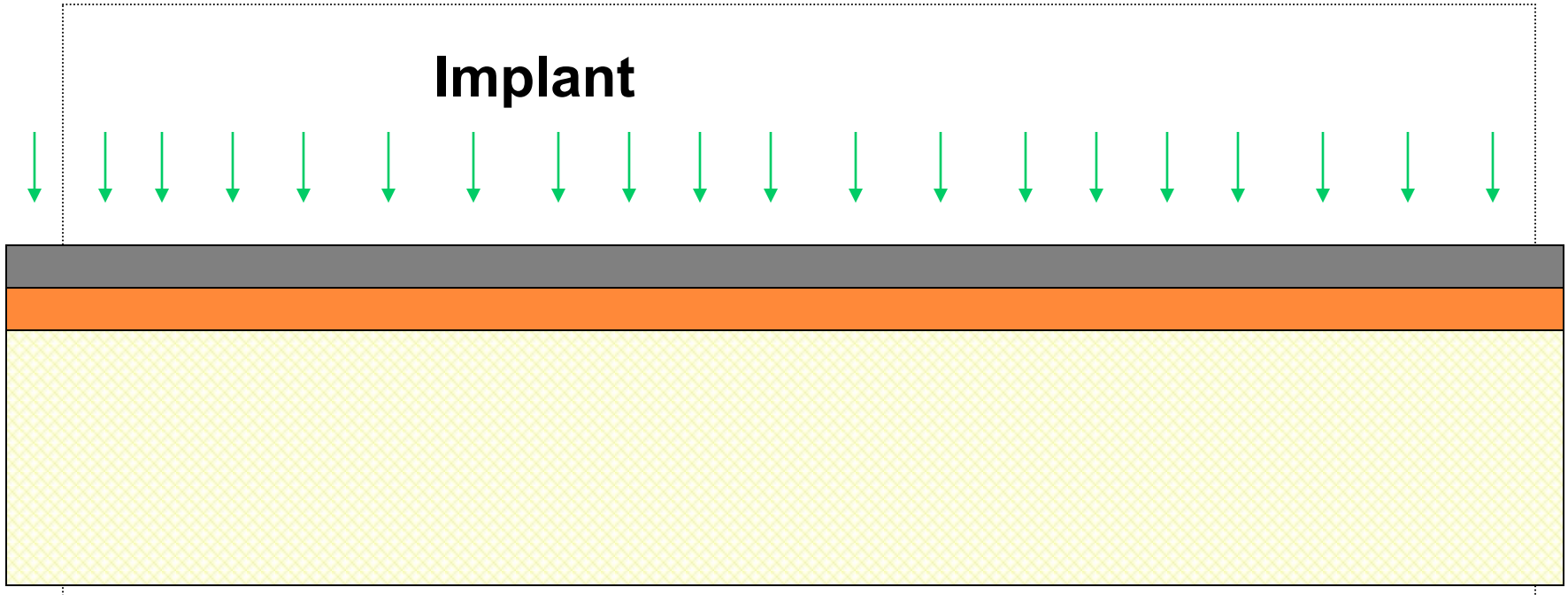
Develop



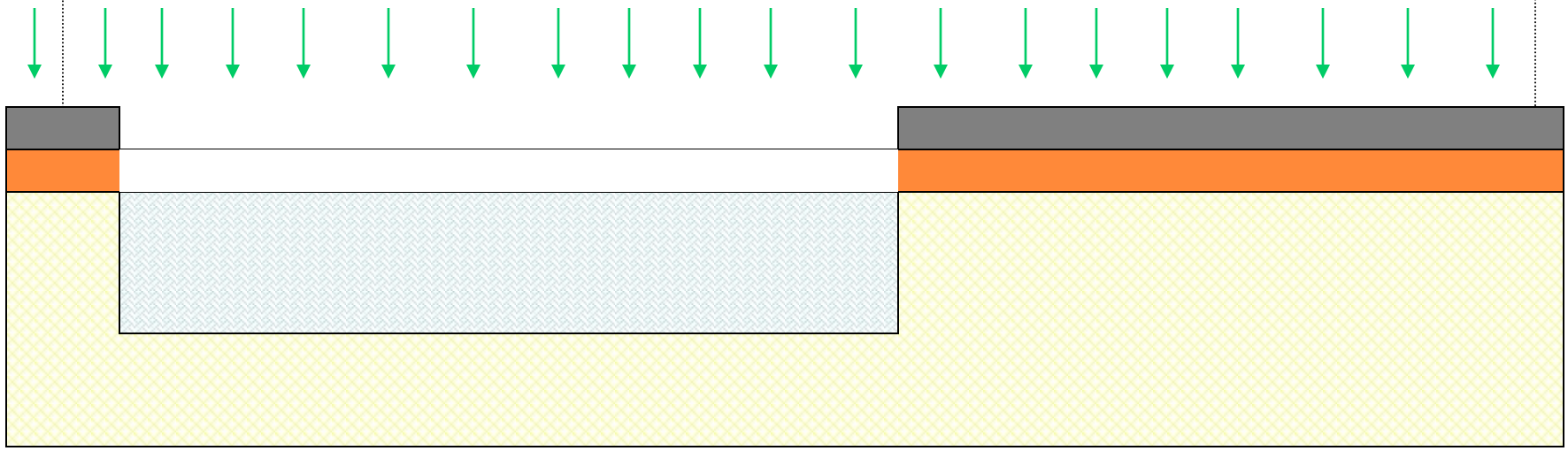
A-A’ Section



B-B’ Section

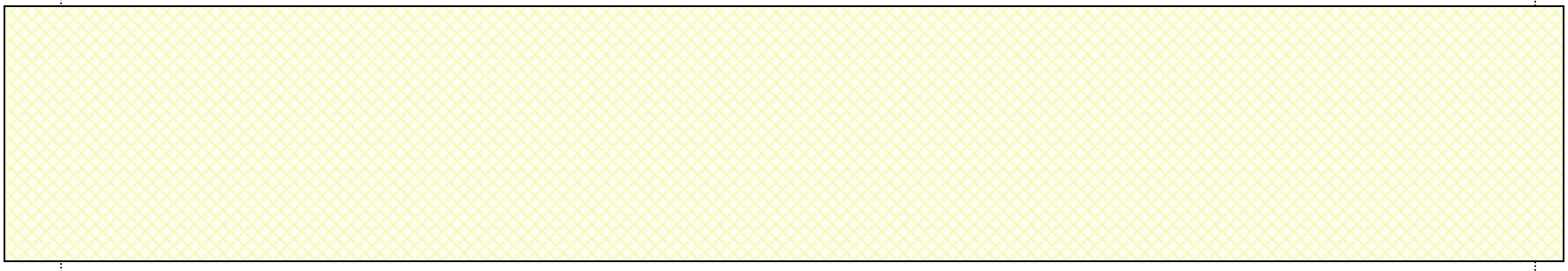


A-A’ Section

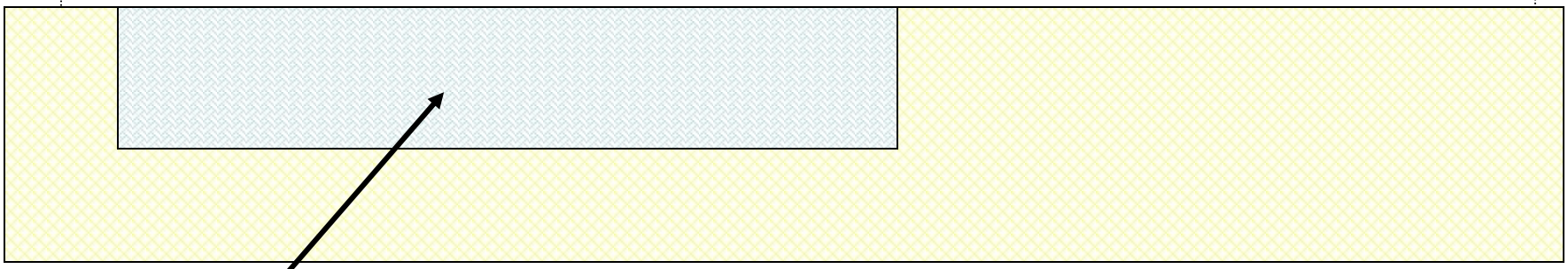


B-B’ Section

N-well Mask



A-A' Section



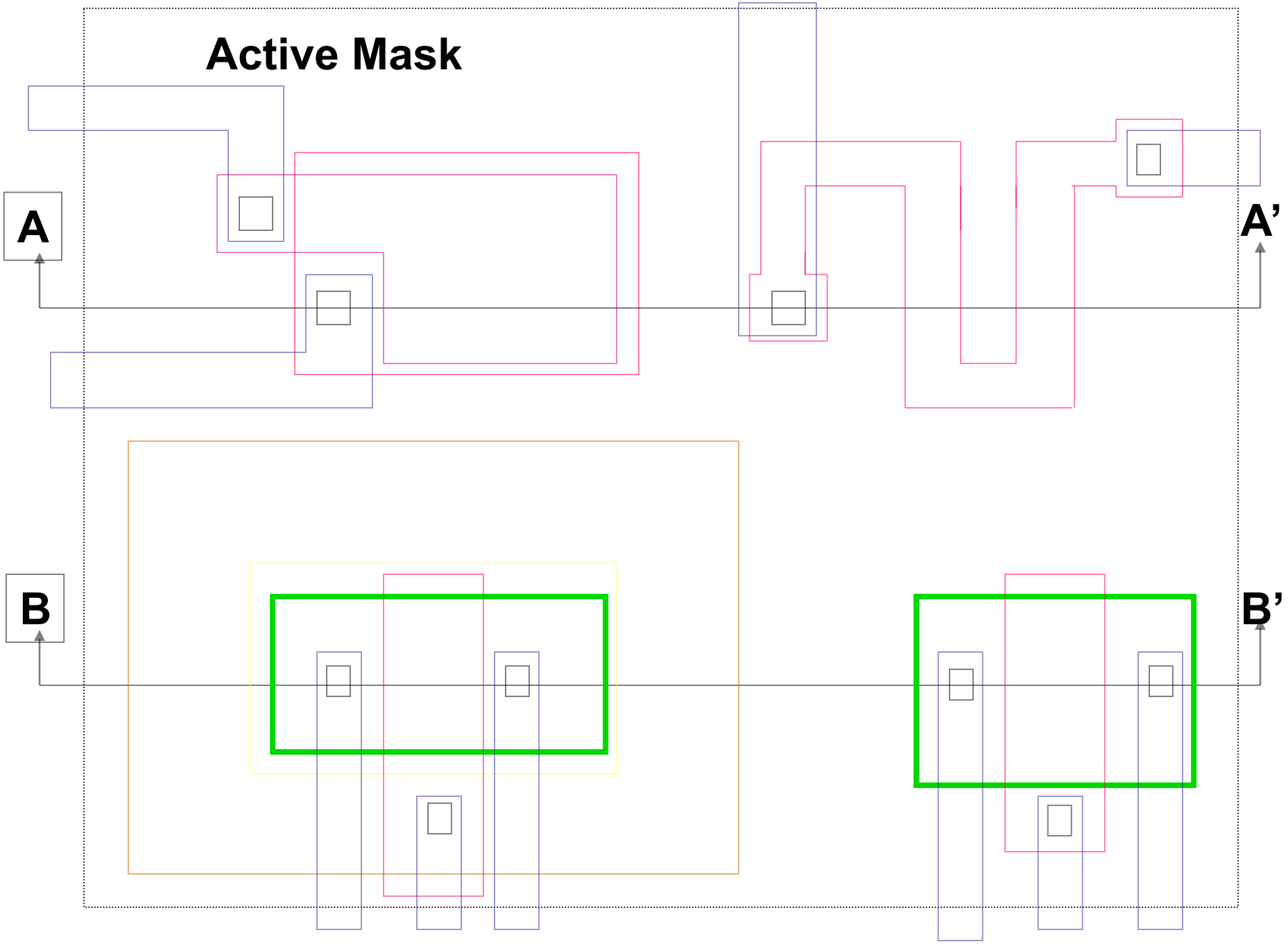
B-B' Section

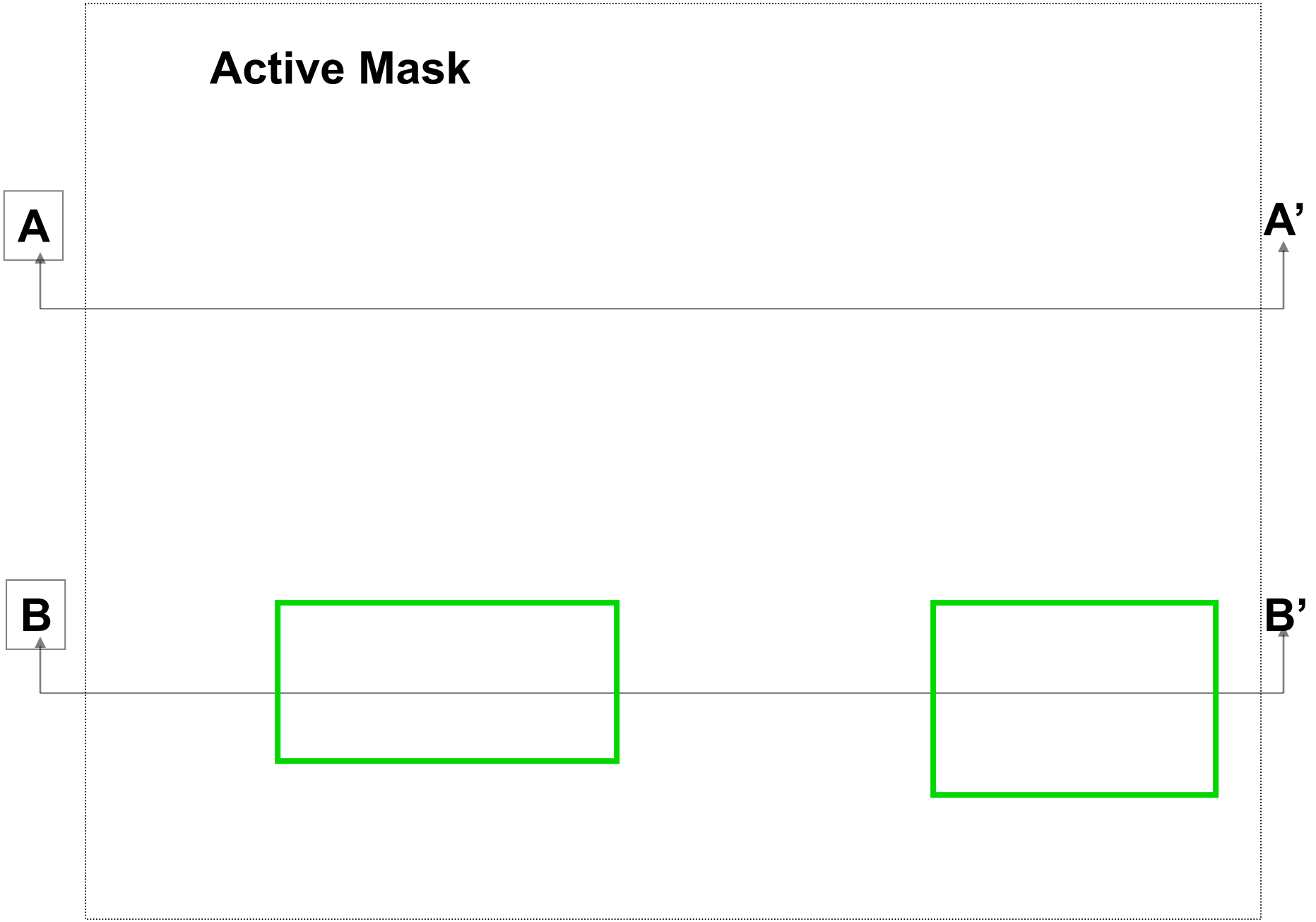
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN **n-well**	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus **n**-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT **p**-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

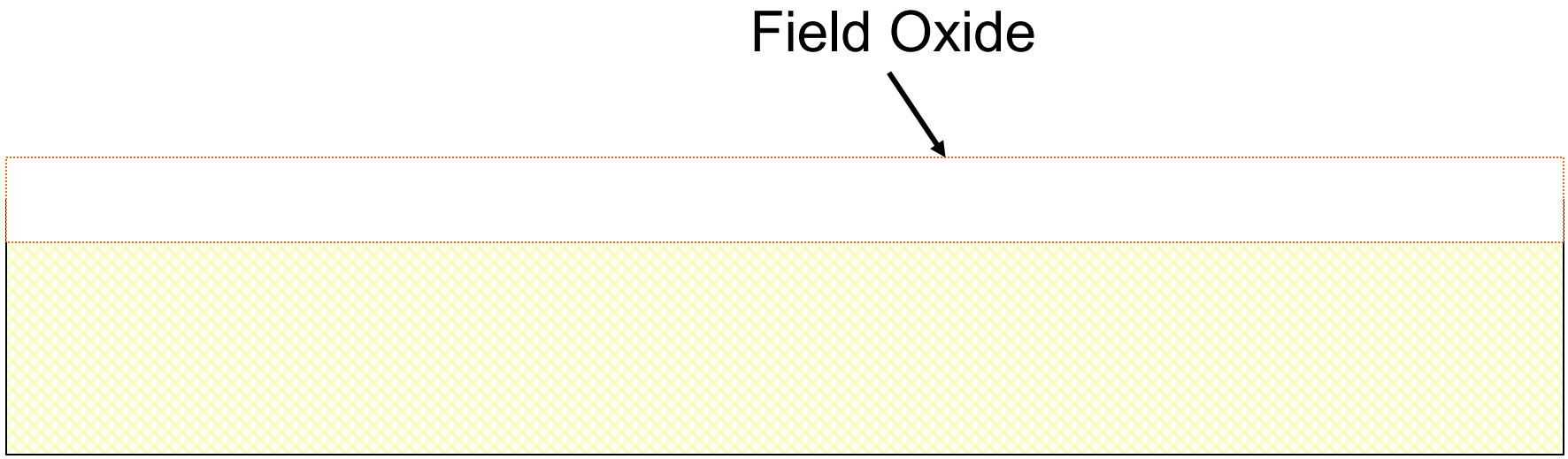
n-well mask

active mask

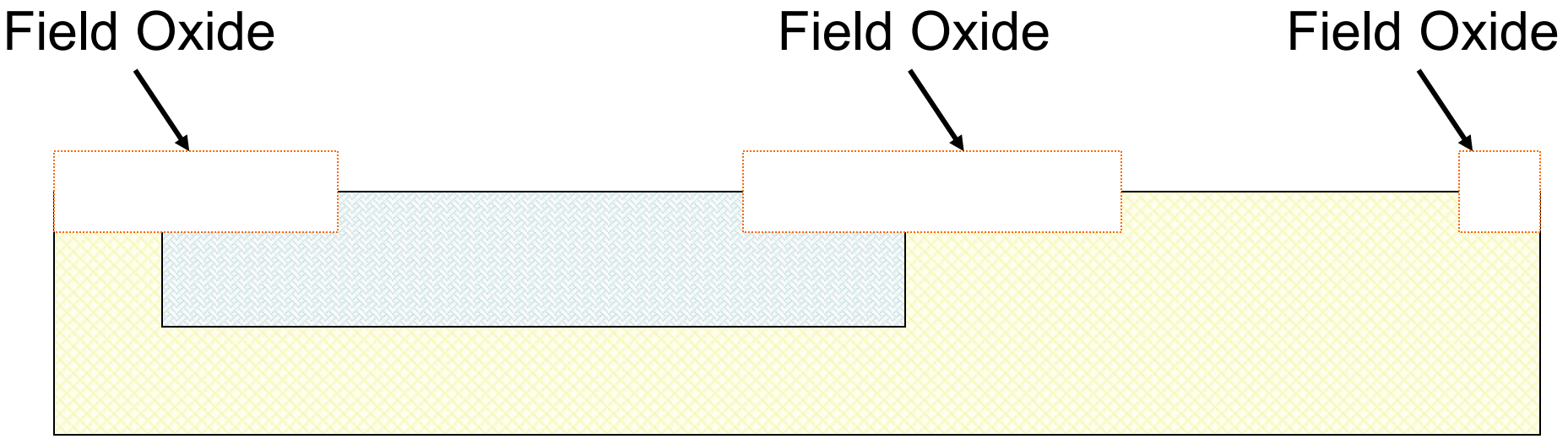

Active Mask
A
A’
B
B’


Active Mask
A
A’
B
B’

Active Mask



A-A' Section



B-B' Section

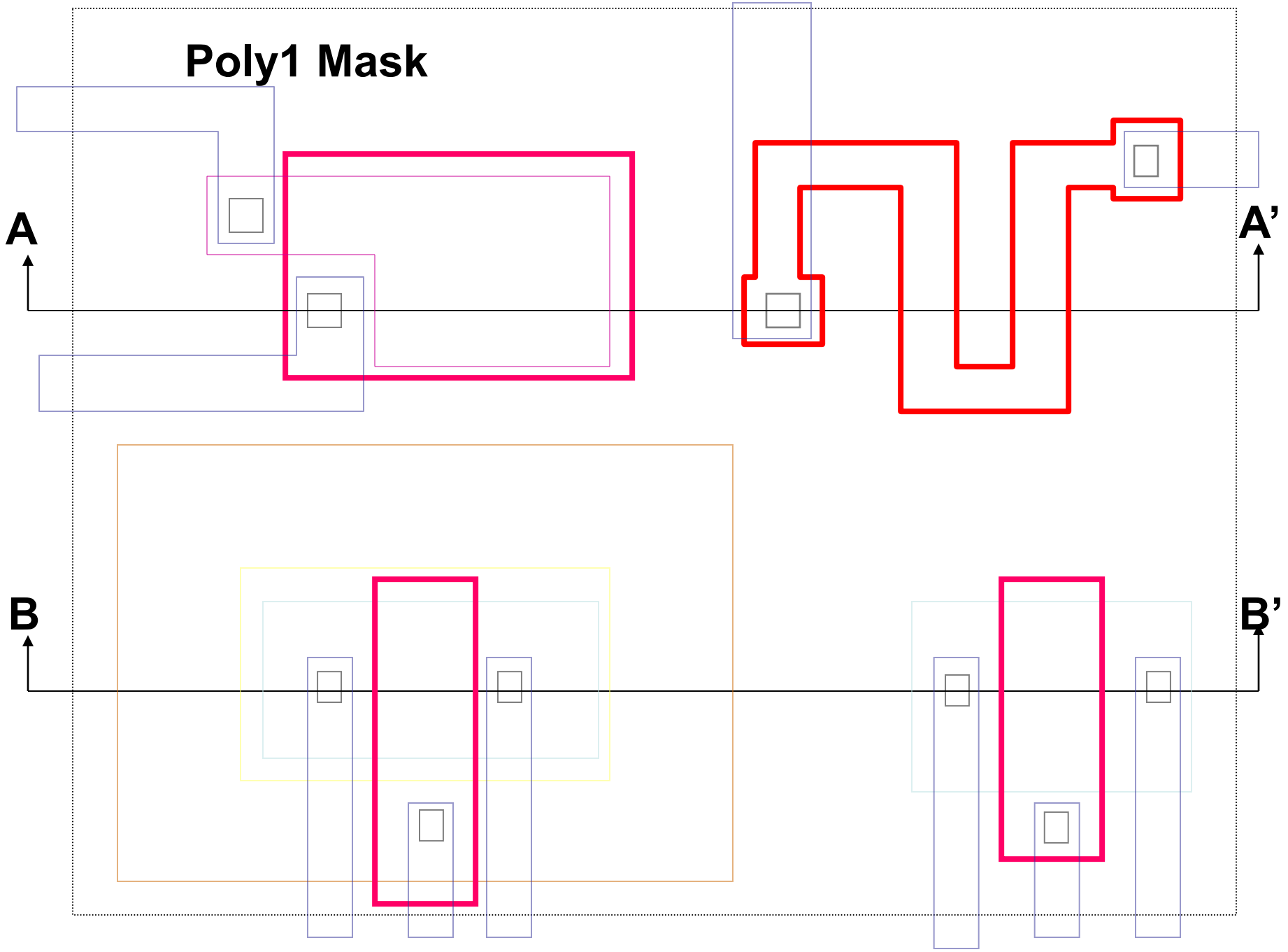
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

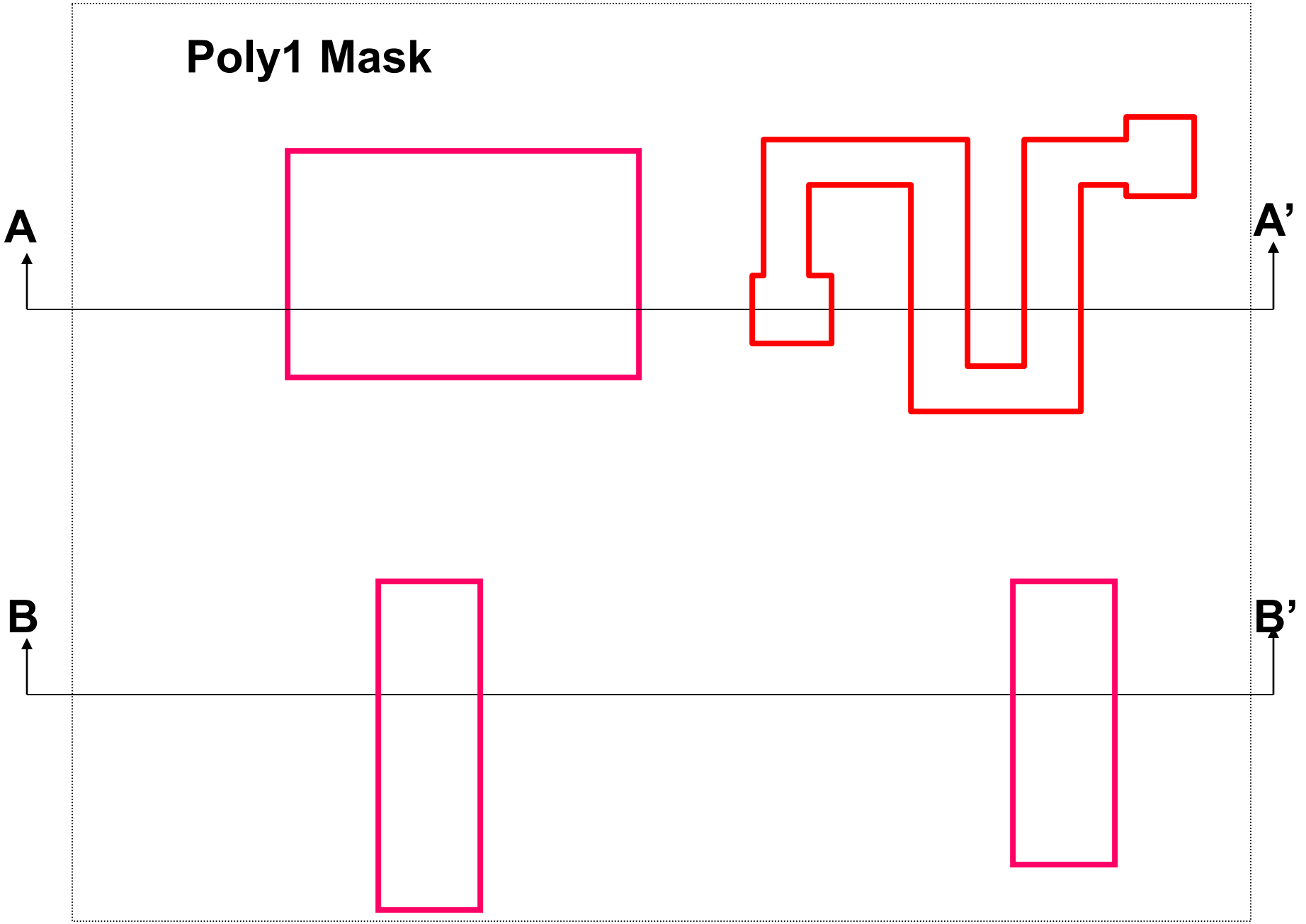
1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN **n-well**	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

n-well mask

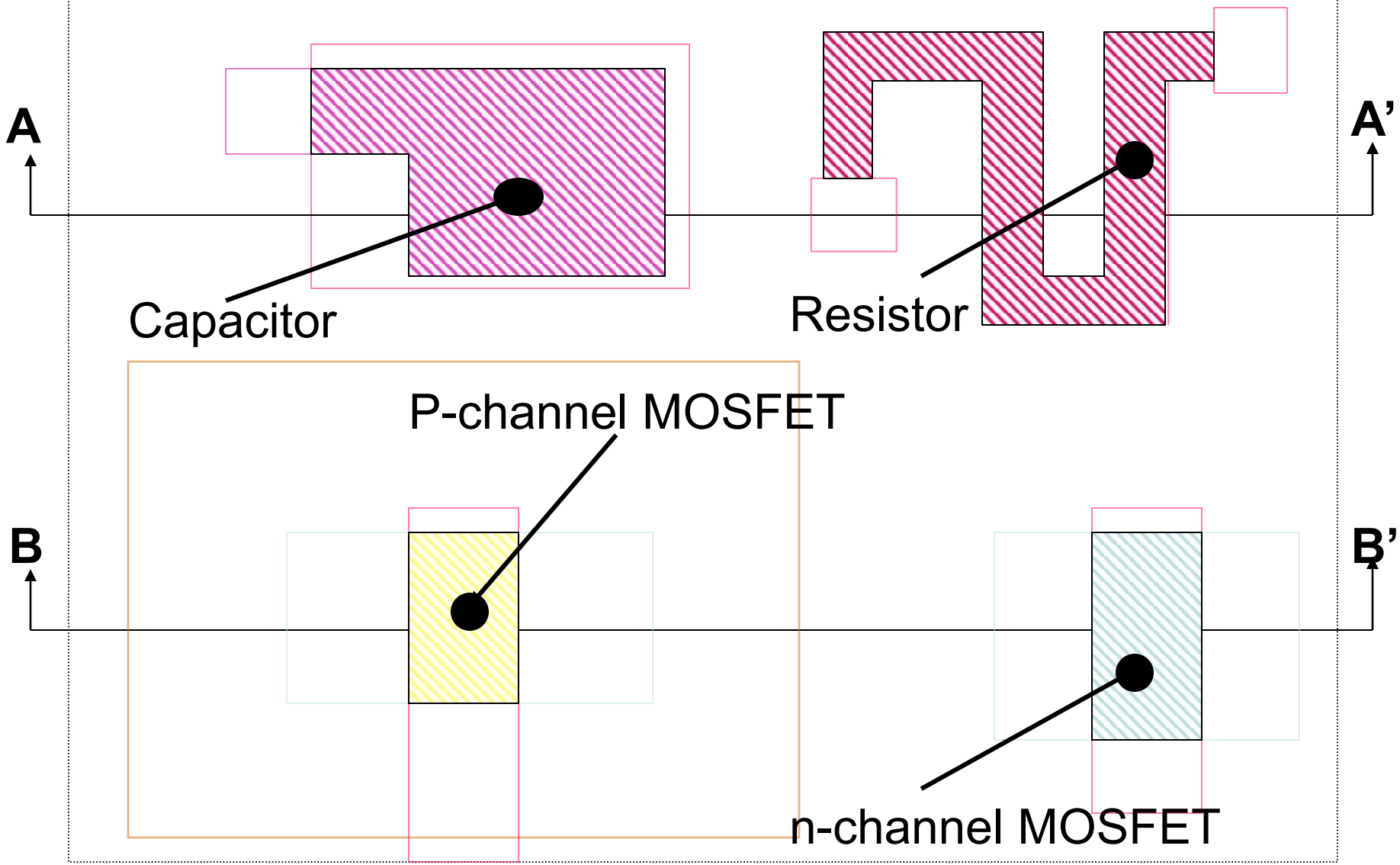
active mask

Poly I mask

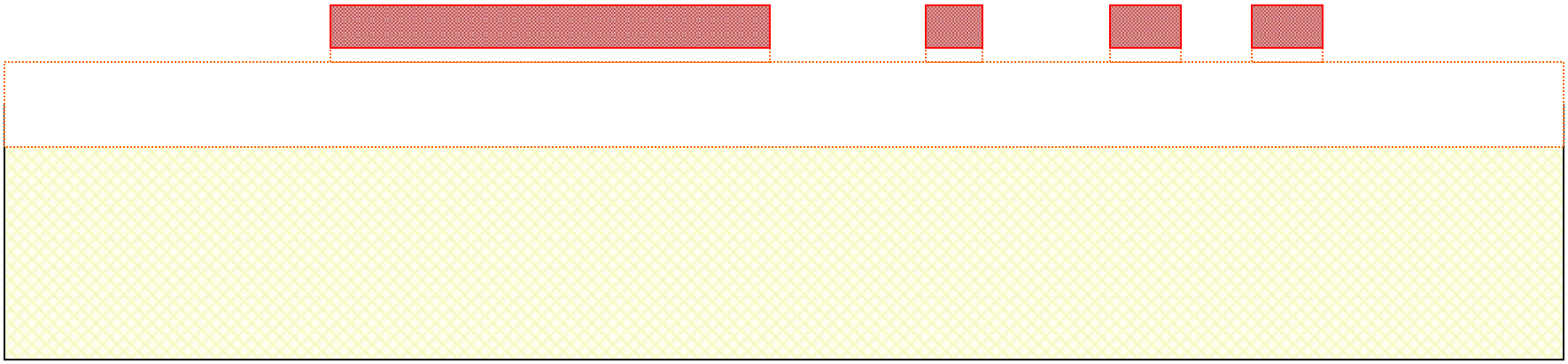

Poly1 Mask
A
A'
B
B'


Poly1 Mask
A
A'
B
B'

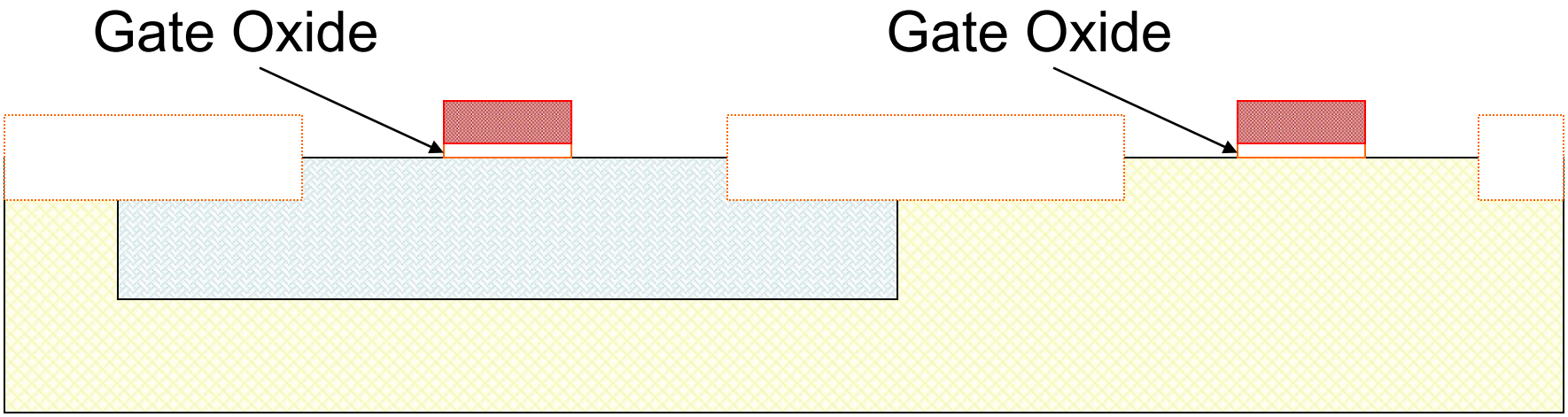
Poly plays a key role in all four types of devices !



Poly 1 Mask



A-A’ Section



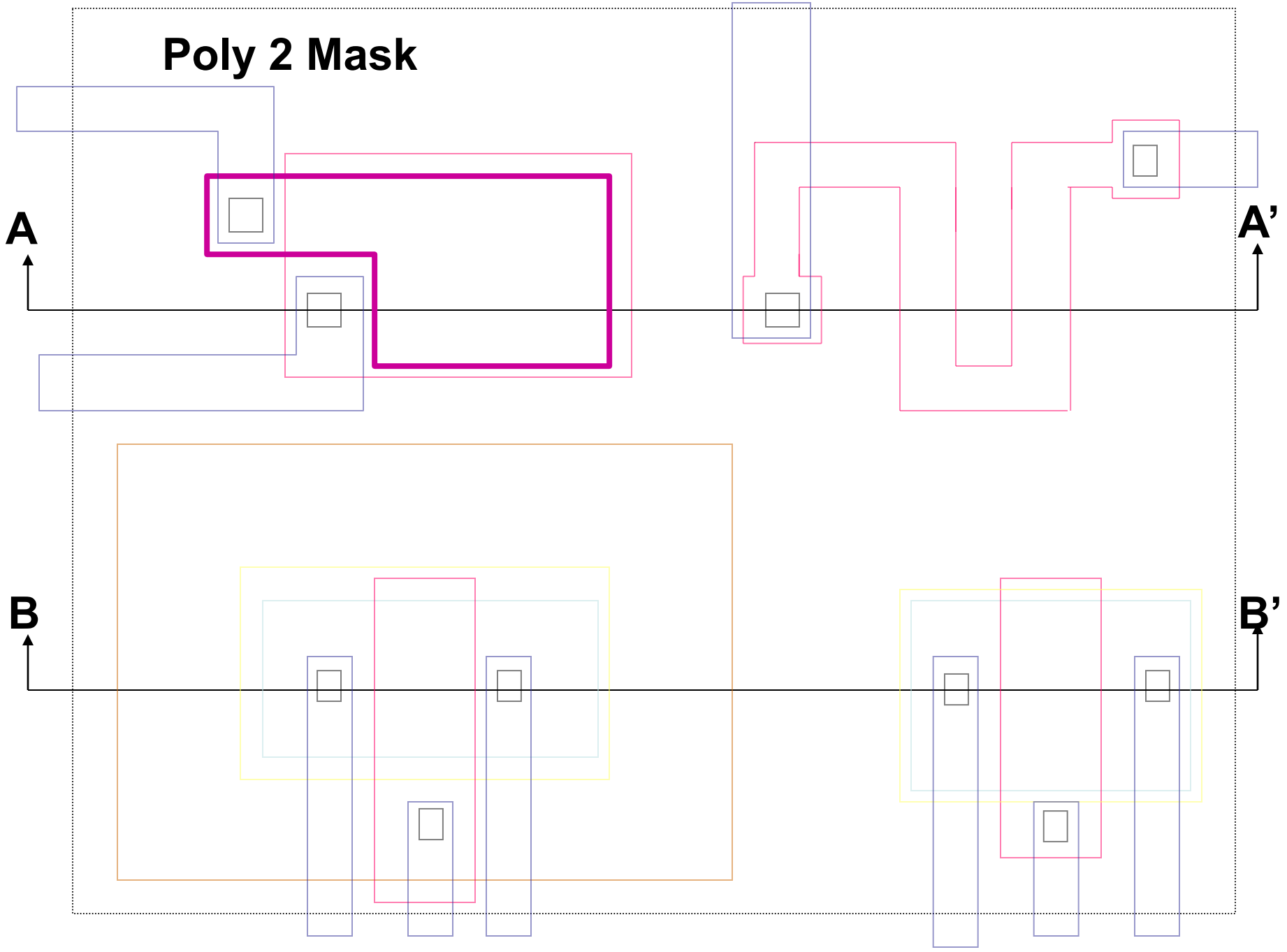
B-B’ Section

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

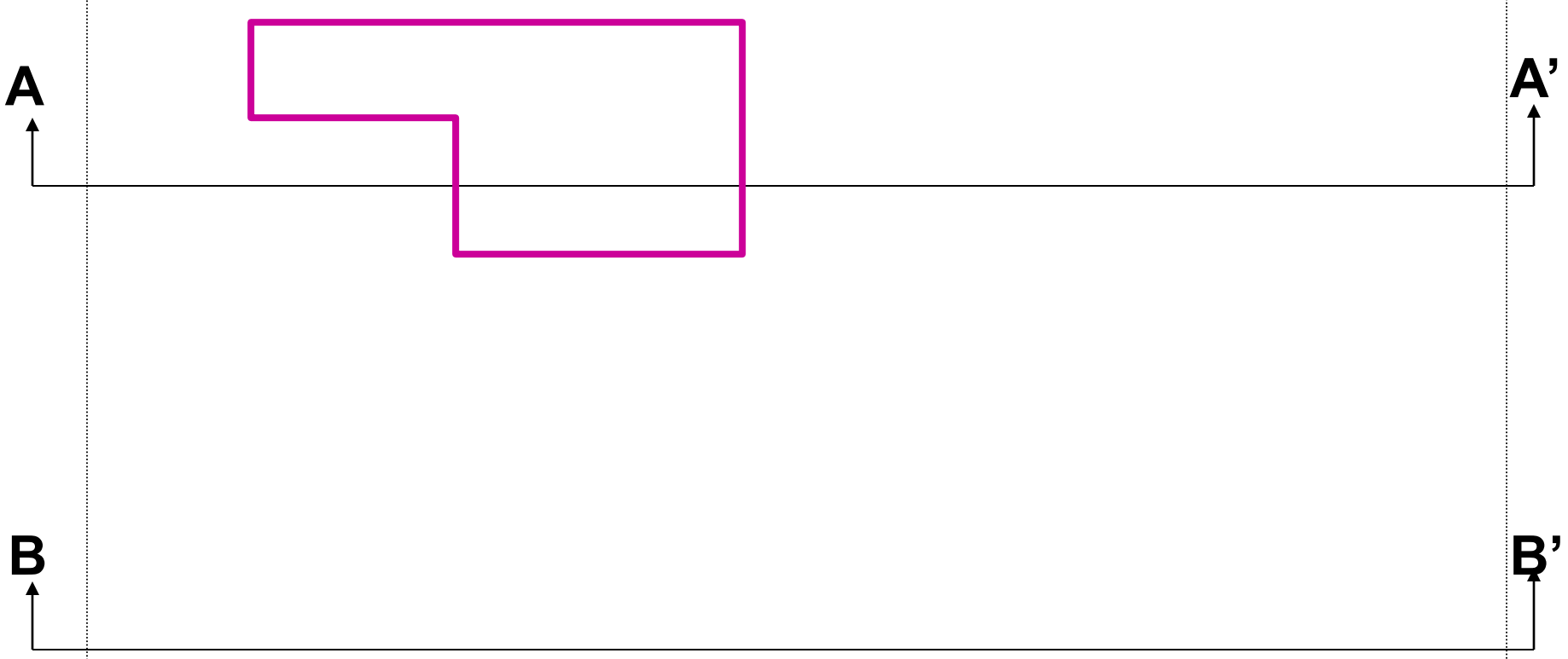
1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25.	Strip photoresist	
	Optional steps for double polysilicon process	
	B.1 Strip thin oxide	
	B.2 GROW THIN OXIDE	
	B.3 POLYSILICON DEPOSITION (POLY II)	
	B.4 Apply photoresist	
	B.5 PATTERN POLYSILICON	(MASK #B1)
	B.6 Develop photoresist	
	B.7 ETCH POLYSILICON	
	B.8 Strip photoresist	
	B.9 Strip thin oxide	
26.	Apply photoresist	
27.	PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts)	(MASK #4)
28.	Develop photoresist	
29.	p^+ IMPLANT	
30.	Strip photoresist	
31.	Apply photoresist	
32.	PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate)	(MASK #5)
33.	Develop photoresist	
34.	n^+ IMPLANT	
35.	Strip photoresist	
36.	Strip thin oxide	
37.	Grow oxide	
38.	Apply photoresist	
39.	PATTERN CONTACT OPENINGS	(MASK #6)
40.	Develop photoresist	
41.	Etch oxide	
42.	Strip photoresist	

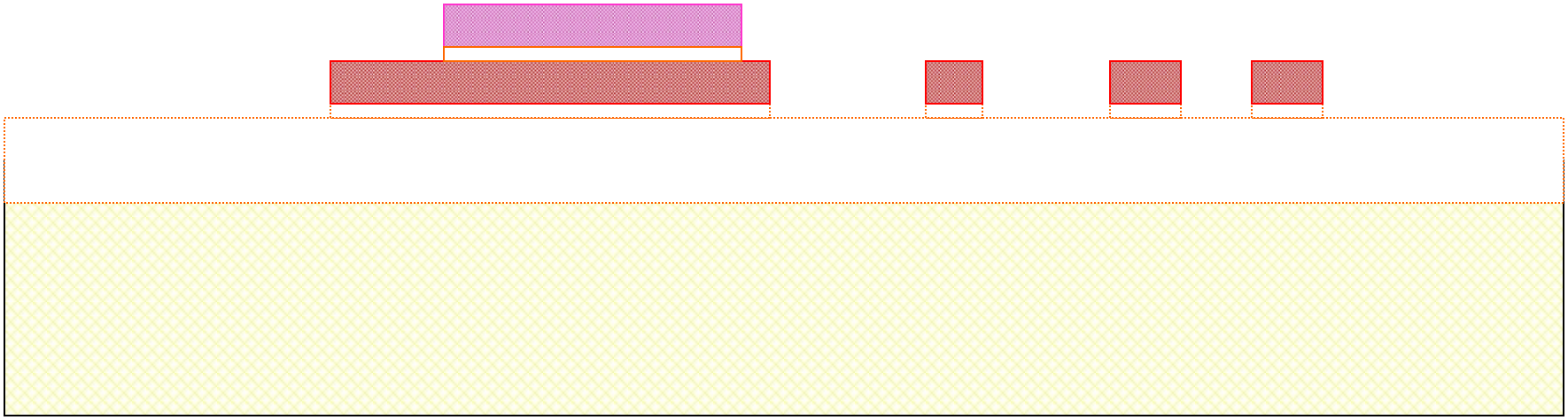
Poly II mask


Poly 2 Mask
A
A'
B
B'

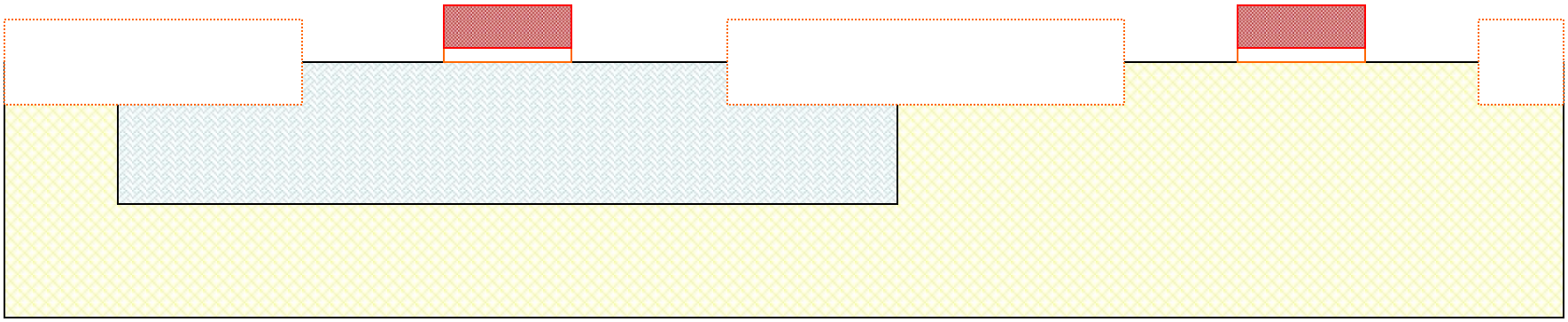
Poly 2 Mask



Poly 2 Mask



A-A’ Section



B-B’ Section

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25. Strip photoresist

Optional steps for double polysilicon process

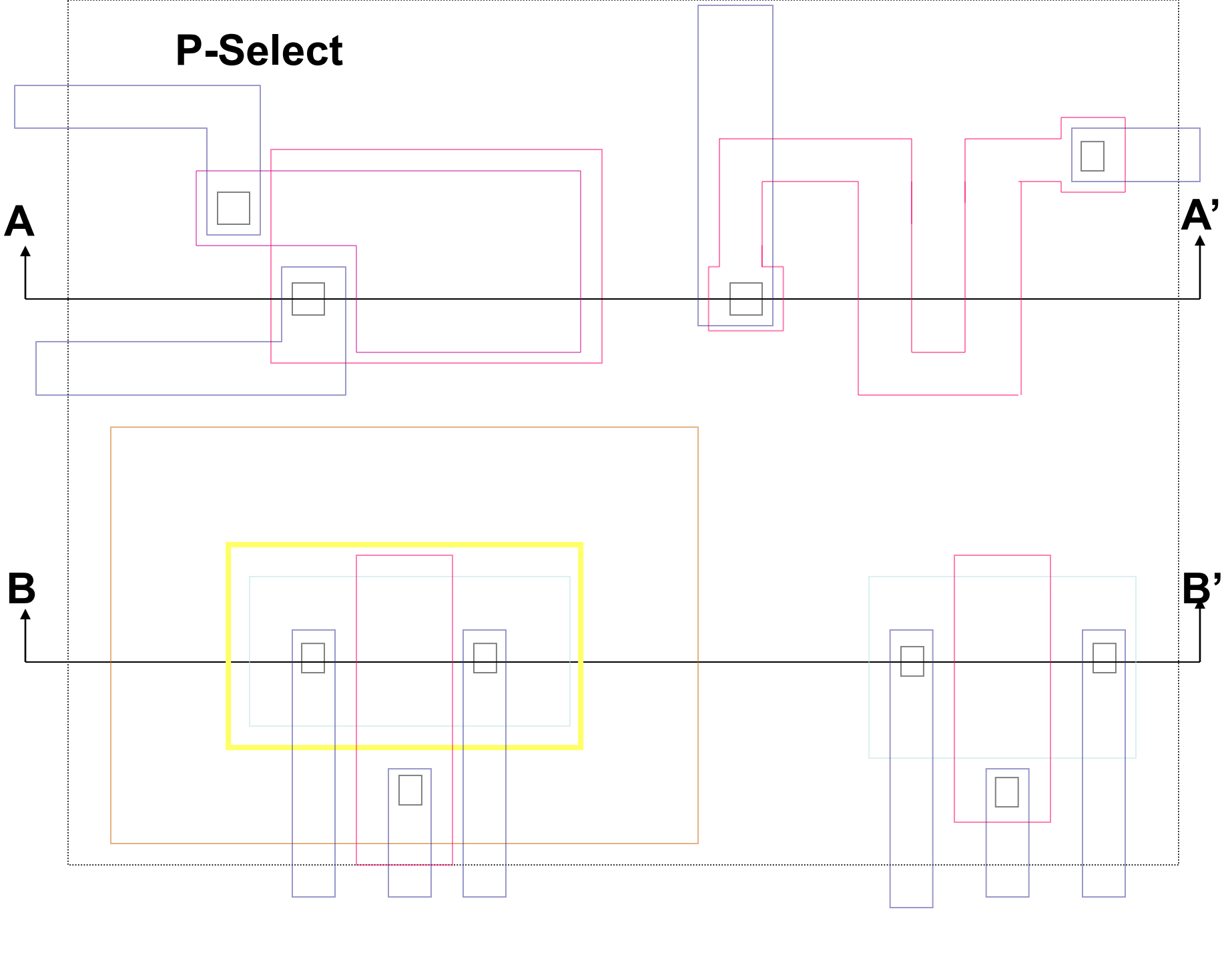
B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

Poly II mask

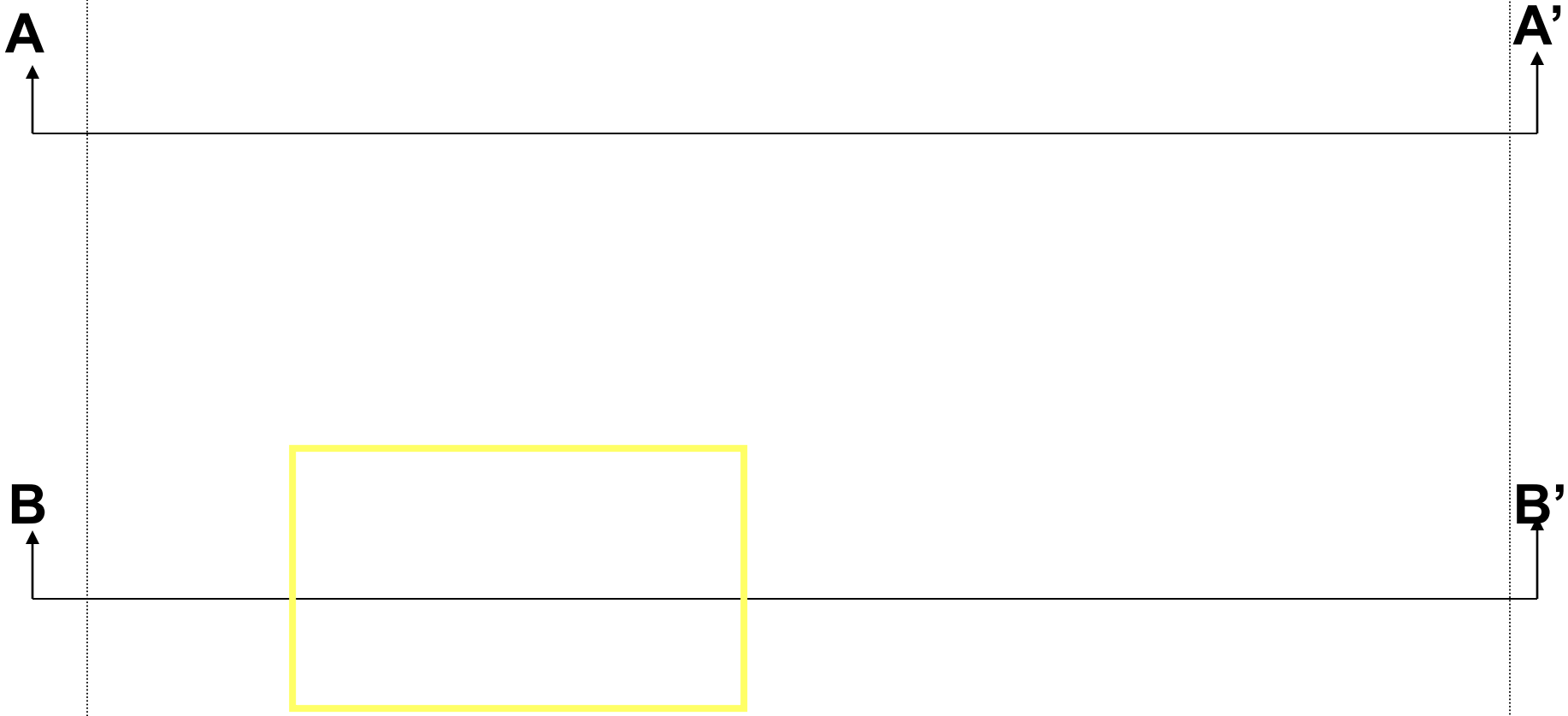
26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist

p-select mask

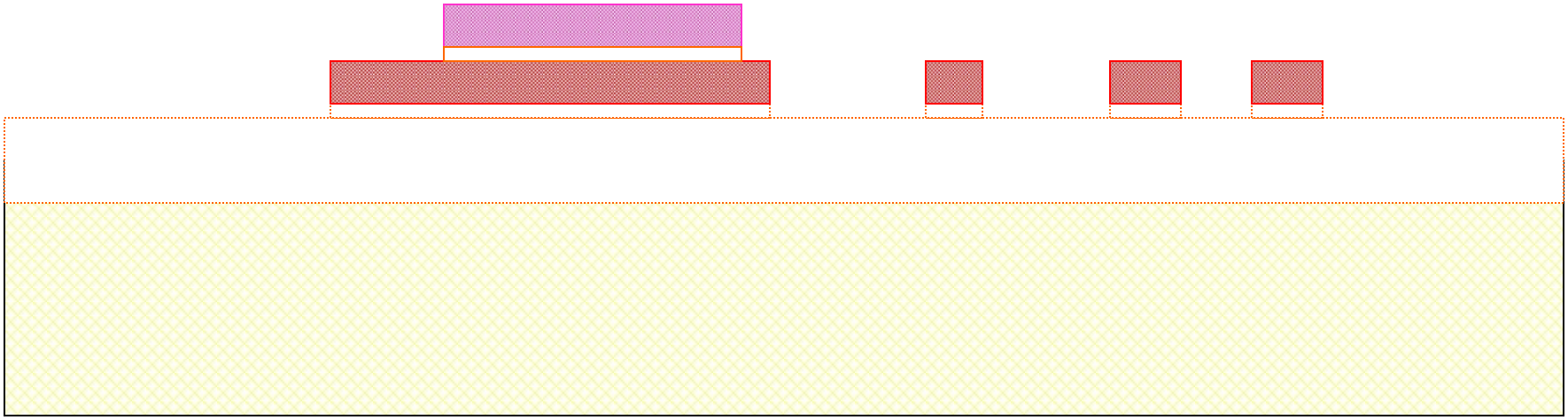
n-select mask


P-Select
A
A'
B
B'

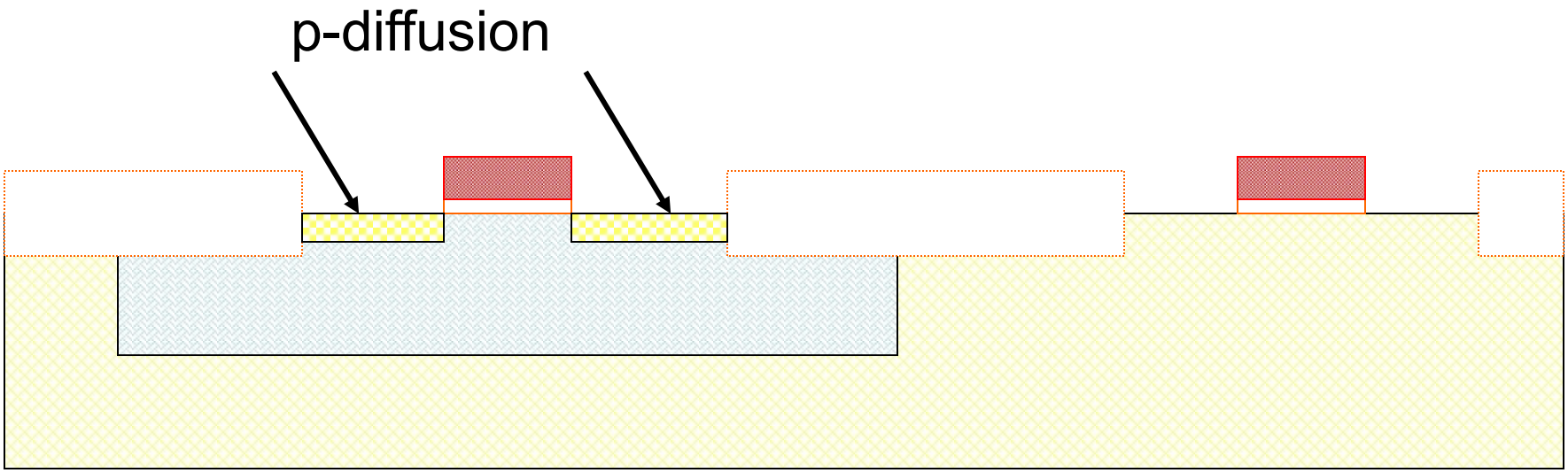
P-Select



P-Select Mask – p-diffusion



A-A' Section

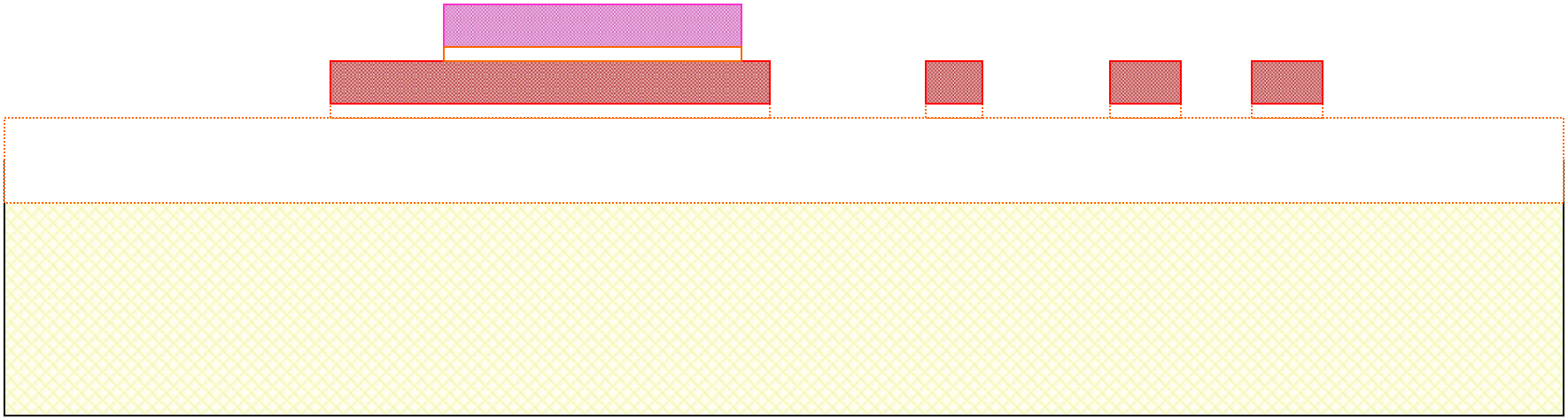


B-B' Section

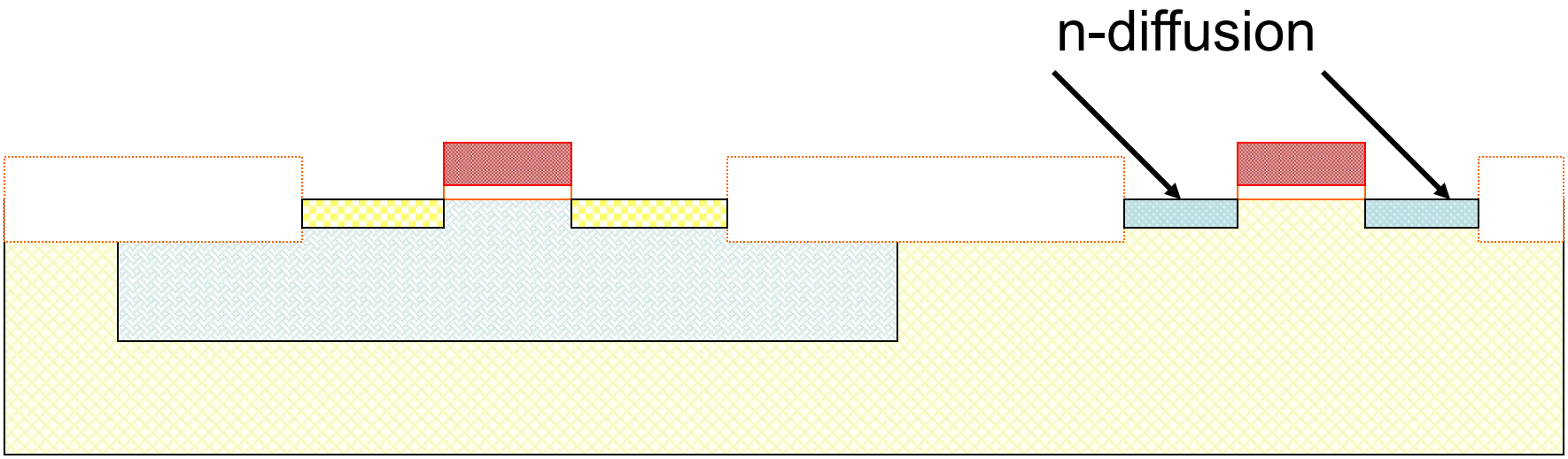
Note the gate is self aligned !!

Note $C_{OXn}=C_{OXp}$!!

n-Select Mask – n-diffusion



A-A’ Section



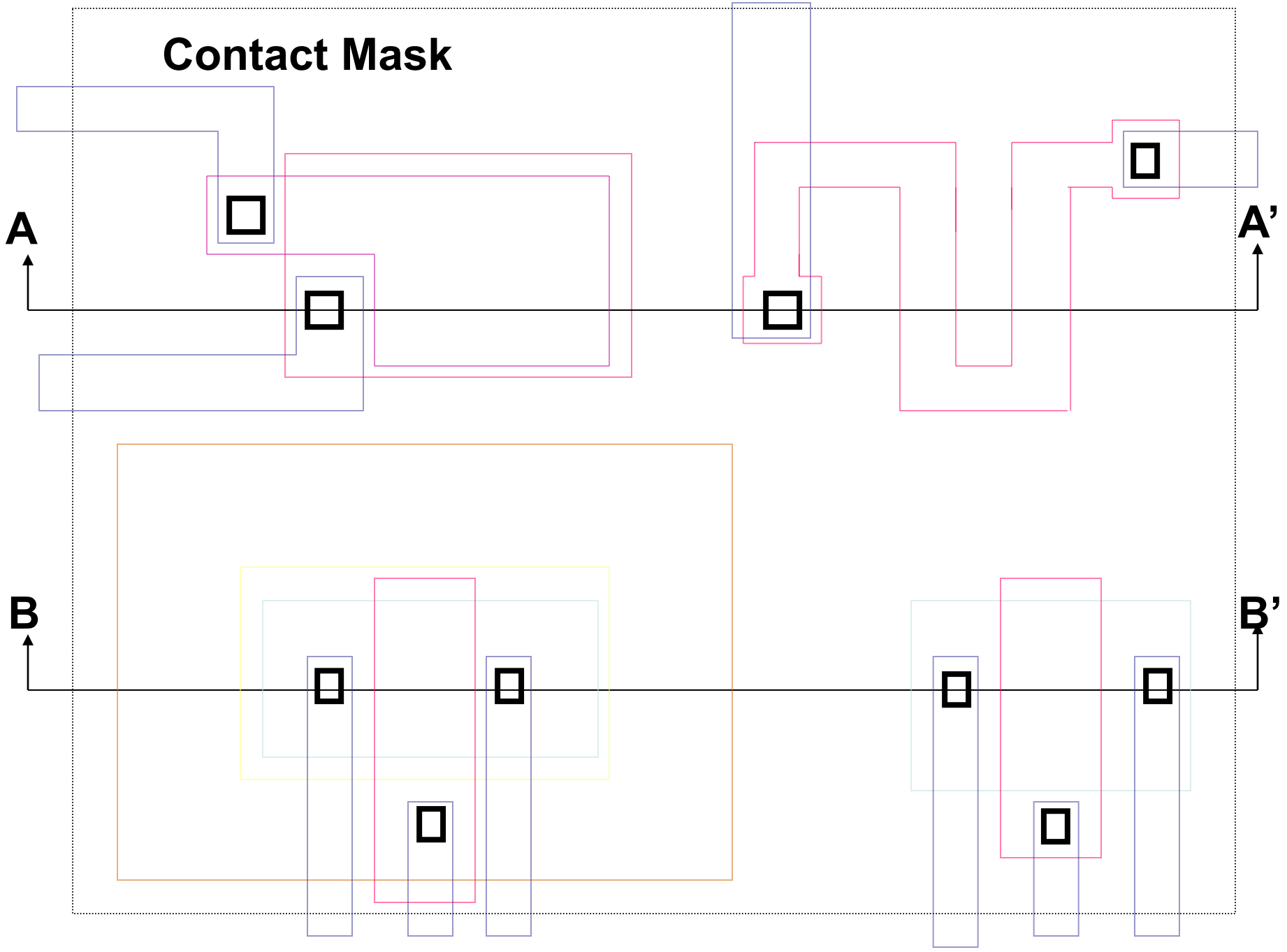
B-B’ Section

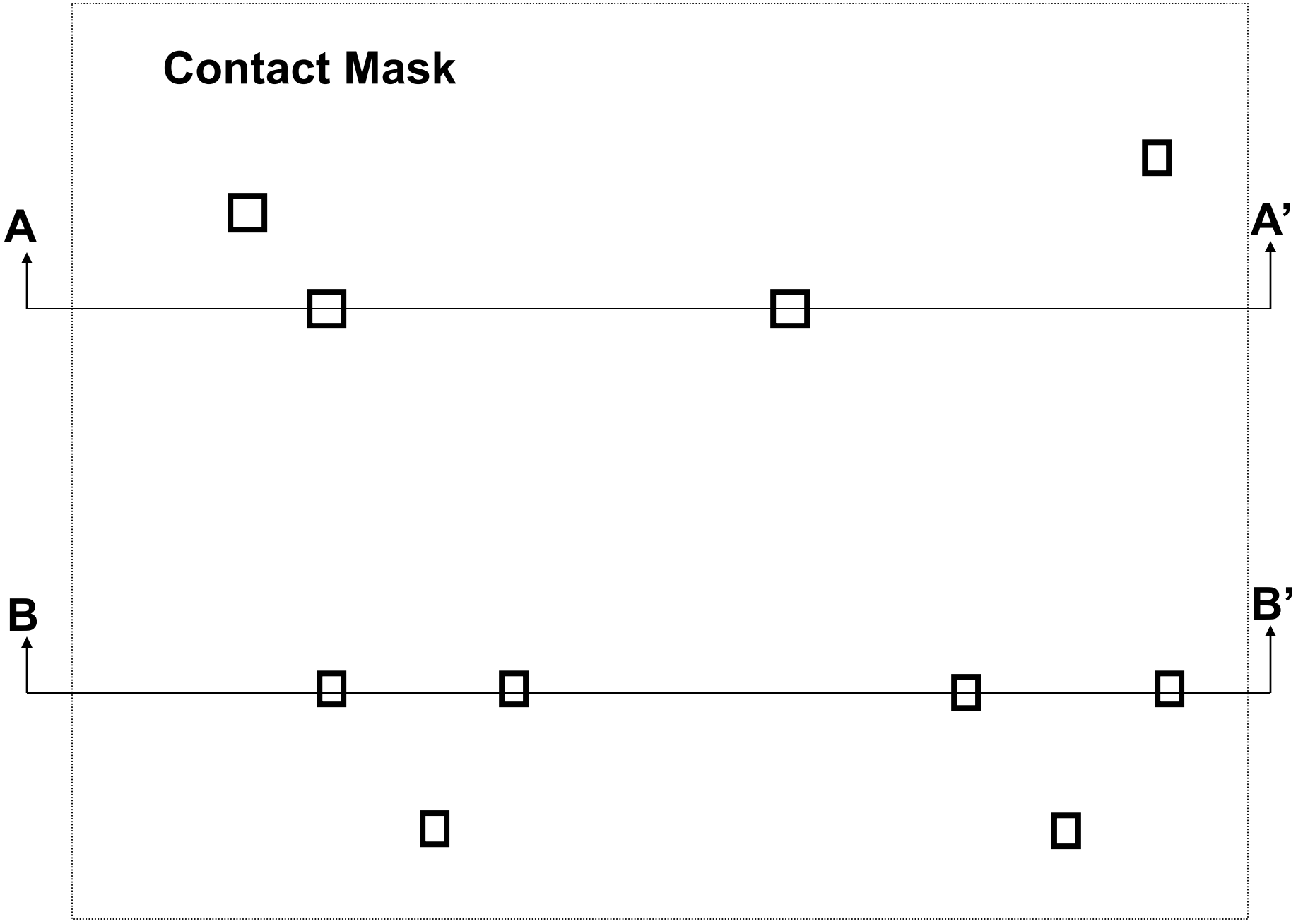
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

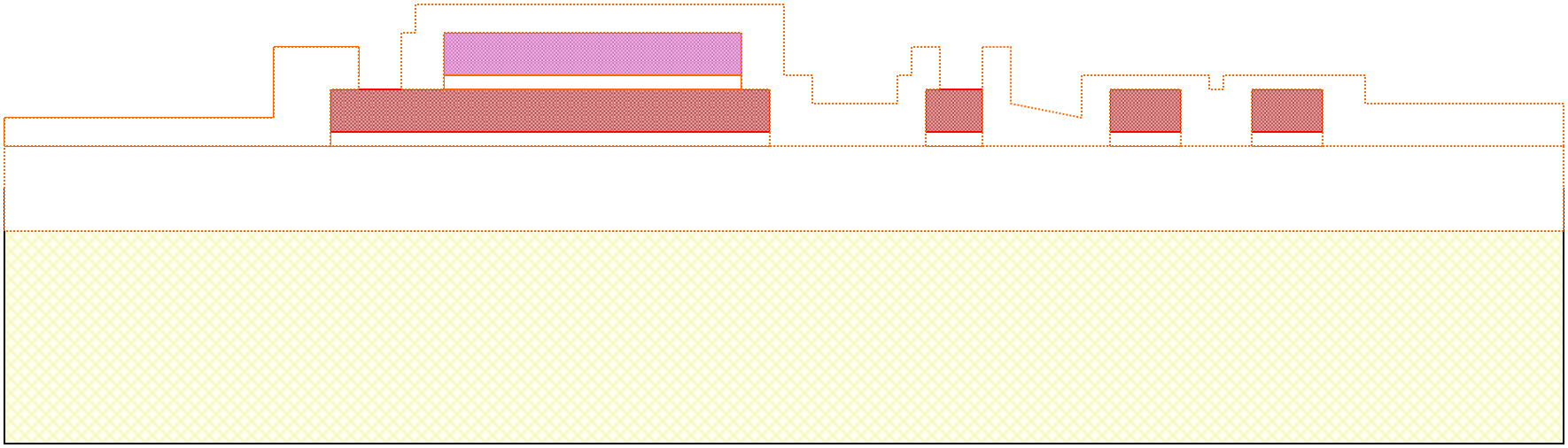
25.	Strip photoresist		
	Optional steps for double polysilicon process		
	B.1 Strip thin oxide		
	B.2 GROW THIN OXIDE		
	B.3 POLYSILICON DEPOSITION (POLY II)		
	B.4 Apply photoresist		
	B.5 PATTERN POLYSILICON	(MASK #B1)	Poly II mask
	B.6 Develop photoresist		
	B.7 ETCH POLYSILICON		
	B.8 Strip photoresist		
	B.9 Strip thin oxide		
26.	Apply photoresist		
27.	PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts)	(MASK #4)	p-select mask
28.	Develop photoresist		
29.	p^+ IMPLANT		
30.	Strip photoresist		
31.	Apply photoresist		
32.	PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate)	(MASK #5)	n-select mask
33.	Develop photoresist		
34.	n^+ IMPLANT		
35.	Strip photoresist		
36.	Strip thin oxide		
37.	Grow oxide		
38.	Apply photoresist		
39.	PATTERN CONTACT OPENINGS	(MASK #6)	contact mask
40.	Develop photoresist		
41.	Etch oxide		
42.	Strip photoresist		

43.	APPLY METAL	
44.	Apply photoresist	
45.	PATTERN METAL	(MASK #7)
46.	Develop photoresist	
47.	Etch metal	
48.	Strip photoresist	
	Optional steps for double metal process	
	C.1 Strip thin oxide	
	C.2 DEPOSIT INTERMETAL OXIDE	
	C.3 Apply photoresist	
	C.4 PATTERN VIAS	(MASK #C1)
	C.5 Develop photoresist	
	C.6 Etch oxide	
	C.7 Strip photoresist	
	C.8 APPLY METAL (Metal 2)	
	C.9 Apply photoresist	
	C.10 PATTERN METAL	(MASK #C2)
	C.11 Develop photoresist	
	C.12 Etch metal	
	C.13 Strip photoresist	
49.	APPLY PASSIVATION	
50.	Apply photoresist	
51.	PATTERN PAD OPENINGS	(MASK #8)
52.	Develop photoresist	
53.	Etch passivation	
54.	Strip photoresist	
55.	ASSEMBLE, PACKAGE AND TEST	

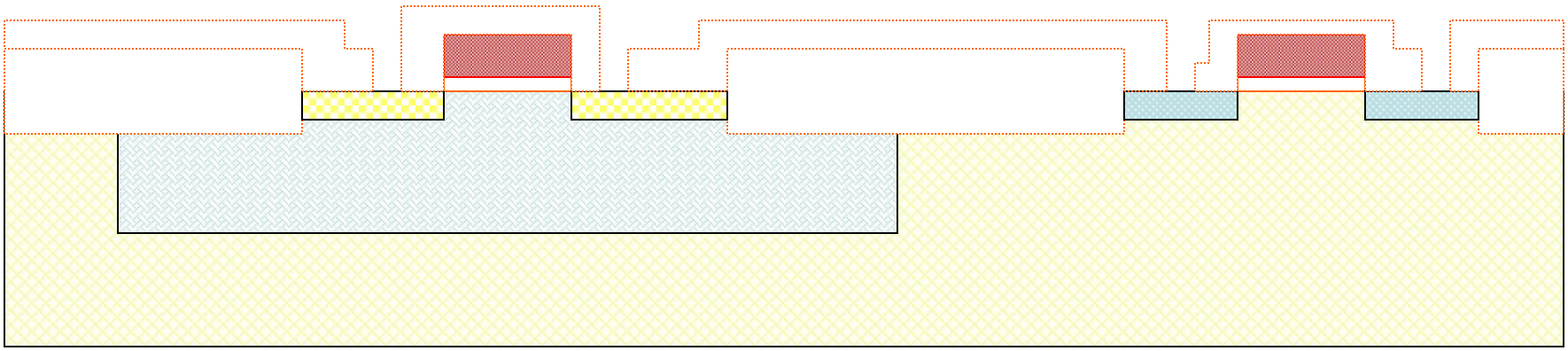

Contact Mask
A
A'
B
B'


Contact Mask
A
A’
B
B’

Contact Mask



A-A’ Section



B-B’ Section

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n-well	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

25. Strip photoresist
Optional steps for double polysilicon process
B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p^+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n^+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist

43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
46. Develop photoresist
47. Etch metal
48. Strip photoresist

Optional steps for double metal process

C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL
C.11 Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

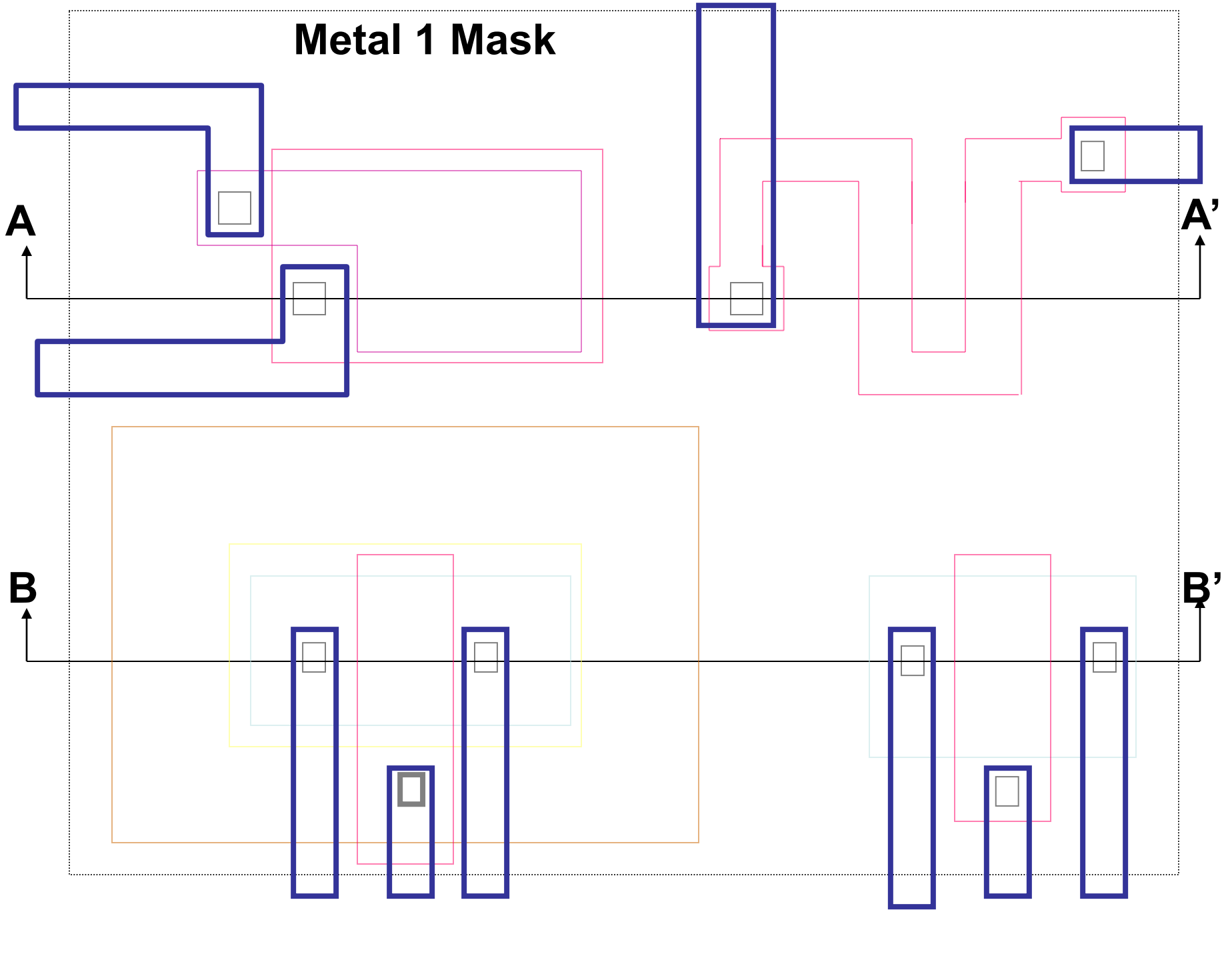
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

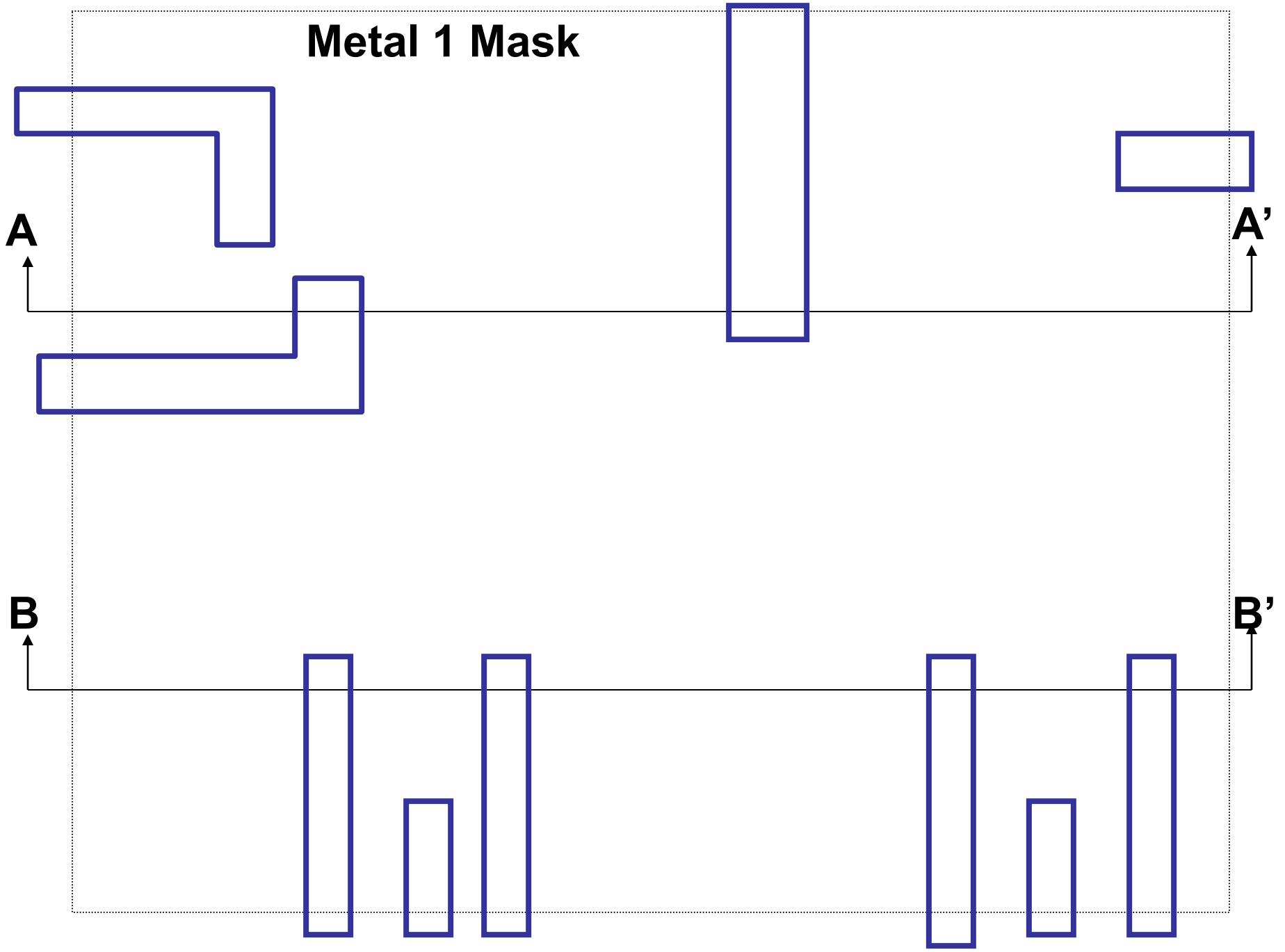
(MASK #7) Metal 1 mask

(MASK #C1) Via mask

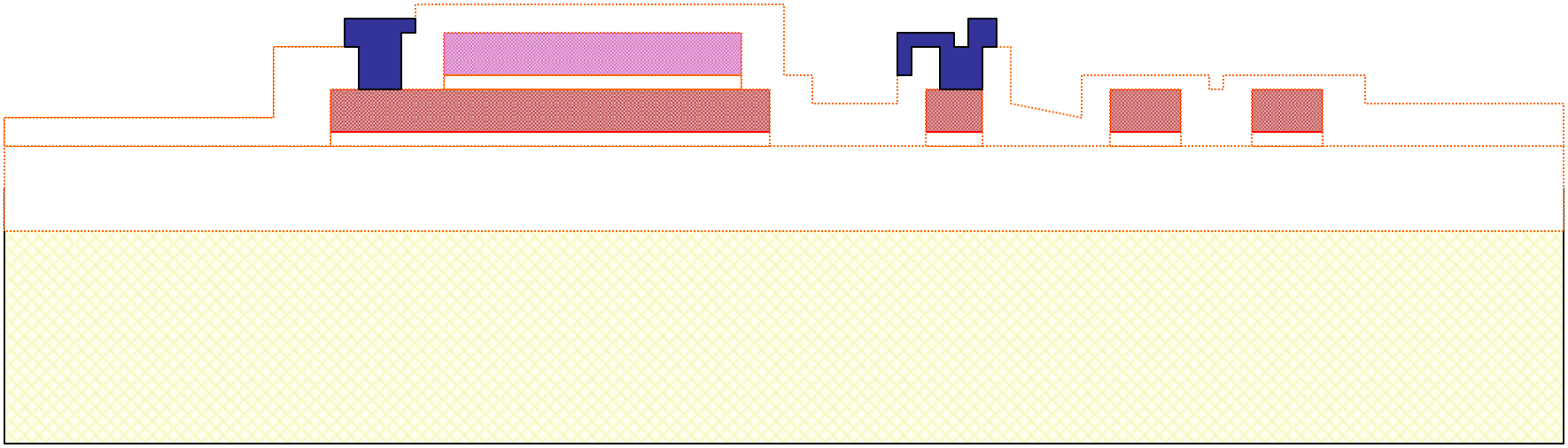
(MASK #C2) Metal 2 mask

(MASK #8) Pad Open mask

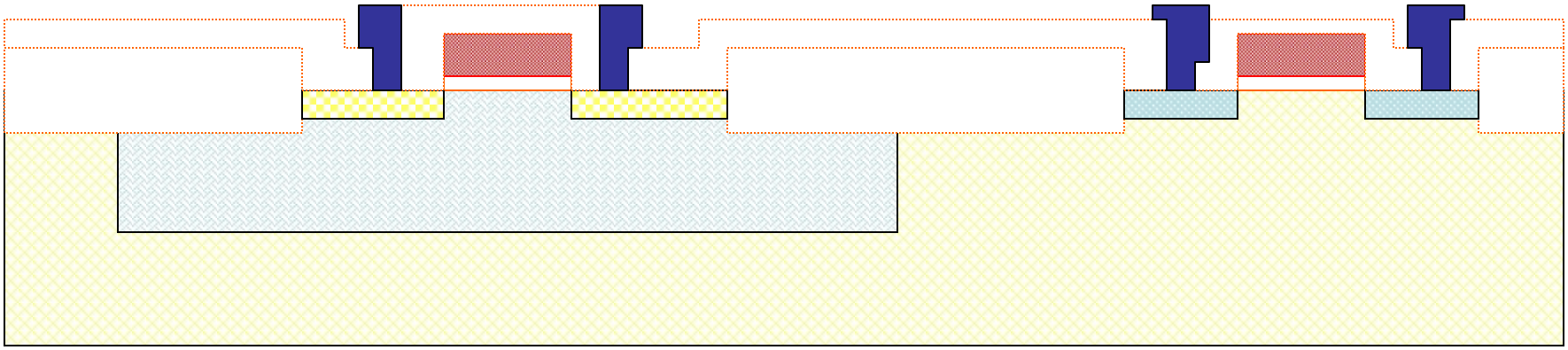

Metal 1 Mask
A
A'
B
B'


Metal 1 Mask
A
A'
B
B'

Metal Mask



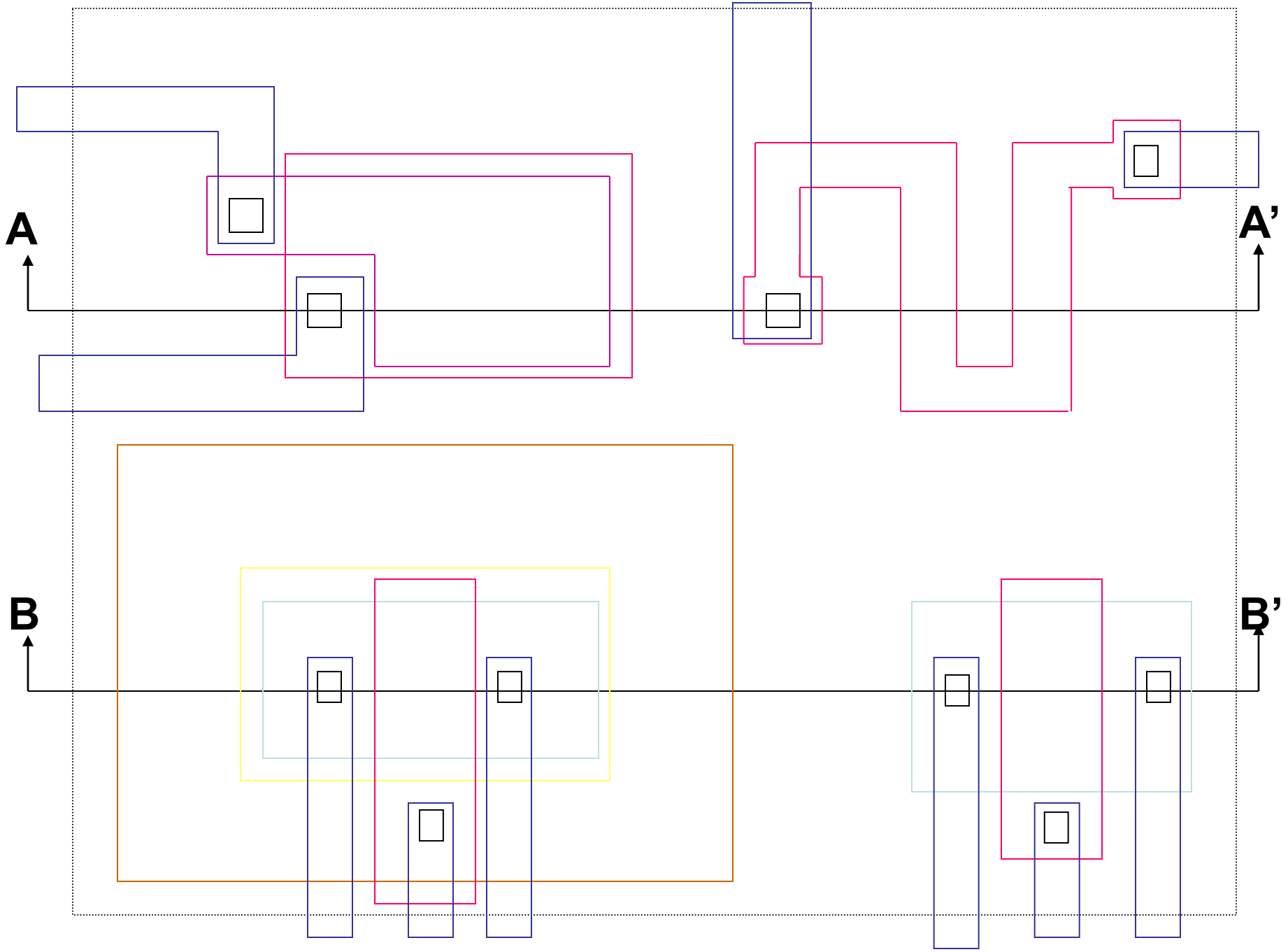
A-A’ Section

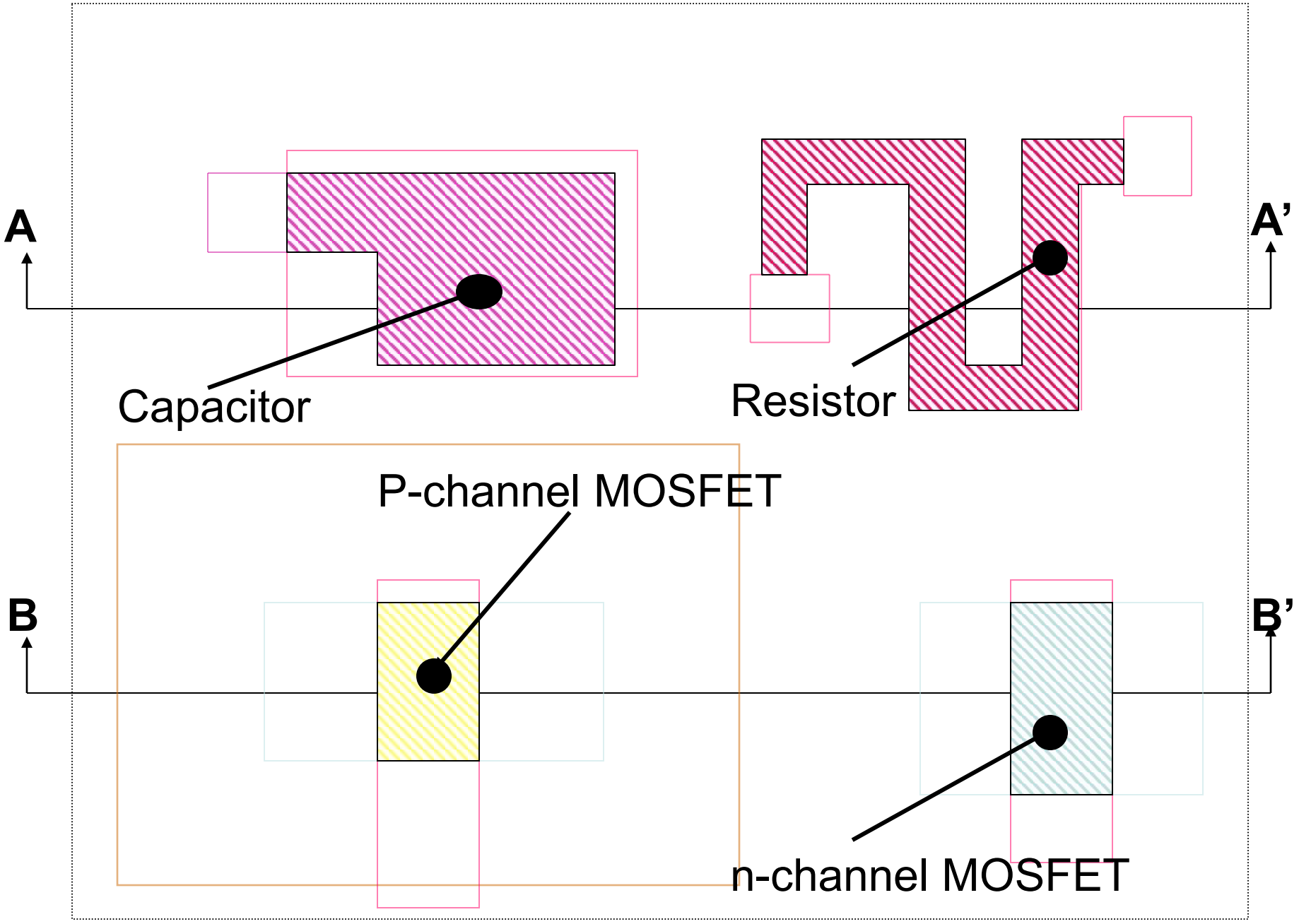


B-B’ Section

Should discuss Metal 2 mask too and mention why we can’t go directly from Metal 2 to active

Should also indicate why, on a multi-metal process that we are restricted from going from one level to another only. Else comments later about what can and can’t be done don’t make any sense.


A
A’
B
B’


A
A'
Capacitor
Resistor
P-channel MOSFET
B
B'
n-channel MOSFET

Should now know what you can do in this process !!

Can metal connect to active?

Can metal connect to substrate when on top of field oxide?

How can metal be connected to substrate?

Can poly be connected to active under gate?

Can poly be connected to active any place?

Can metal be placed under poly to isolate it from bulk?

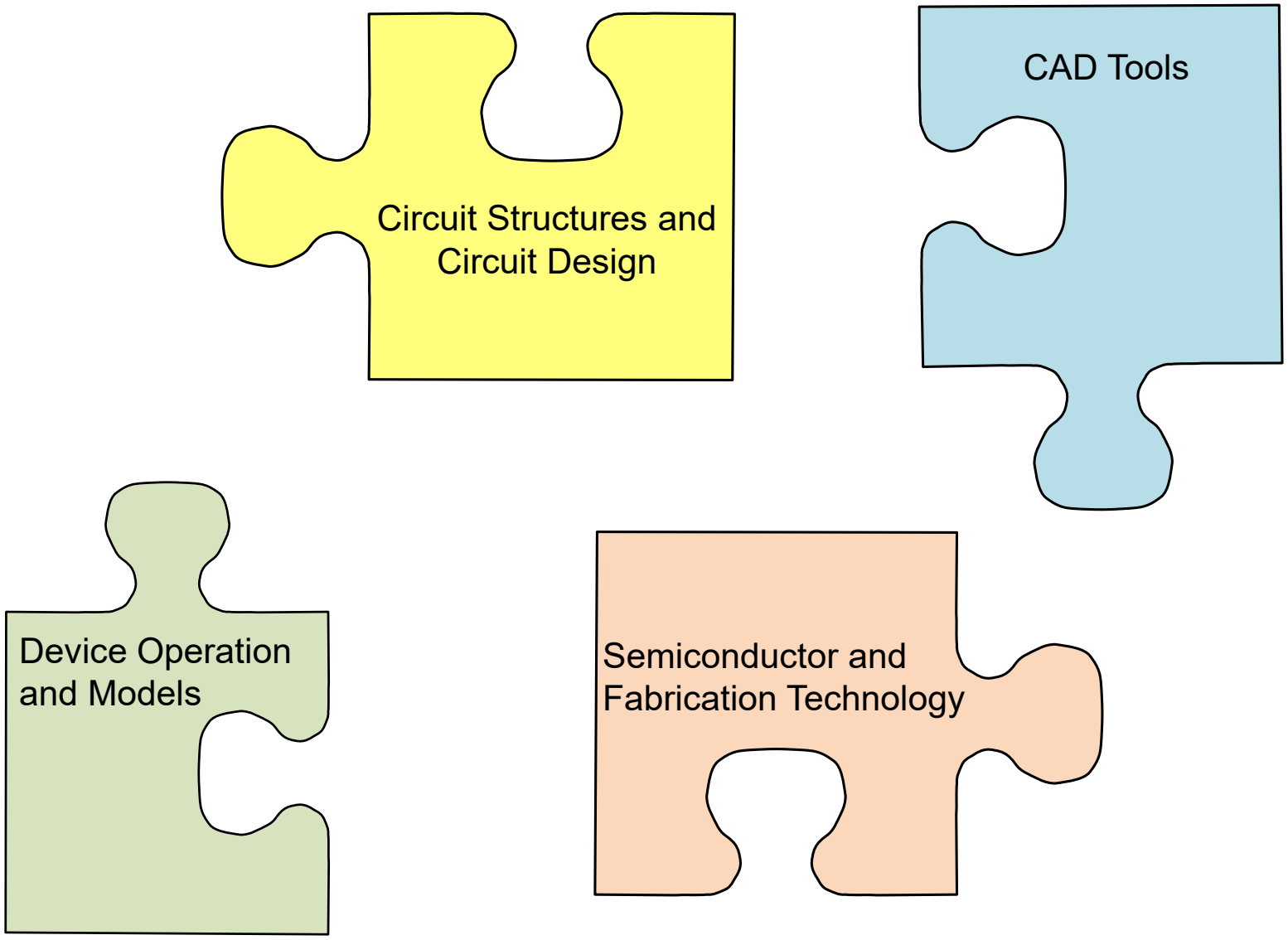
Can metal 2 be connected directly to active?

Can metal 2 be connected to metal 1?

Can metal 2 pass under metal 1?

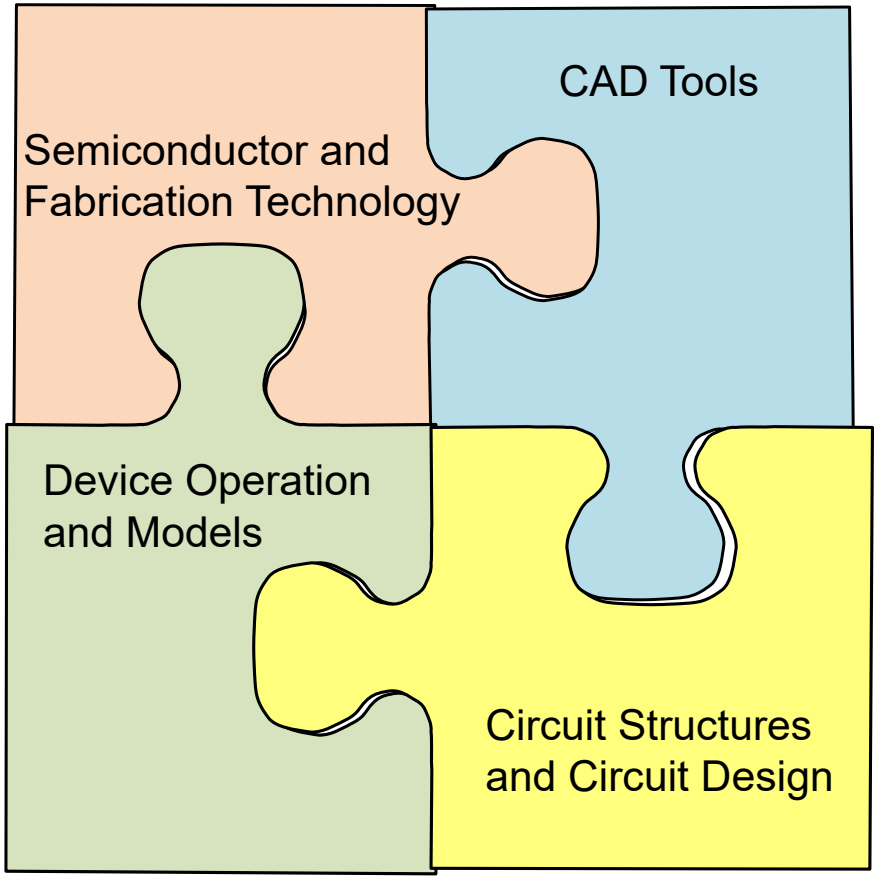
Could a process be created that will result in an answer of YES to most of above?

How we started this course



Thanks for your patience !!

The basic concepts should have now come together



Stay Safe and Stay Healthy !

End of Lecture 18